

# Channel Routing

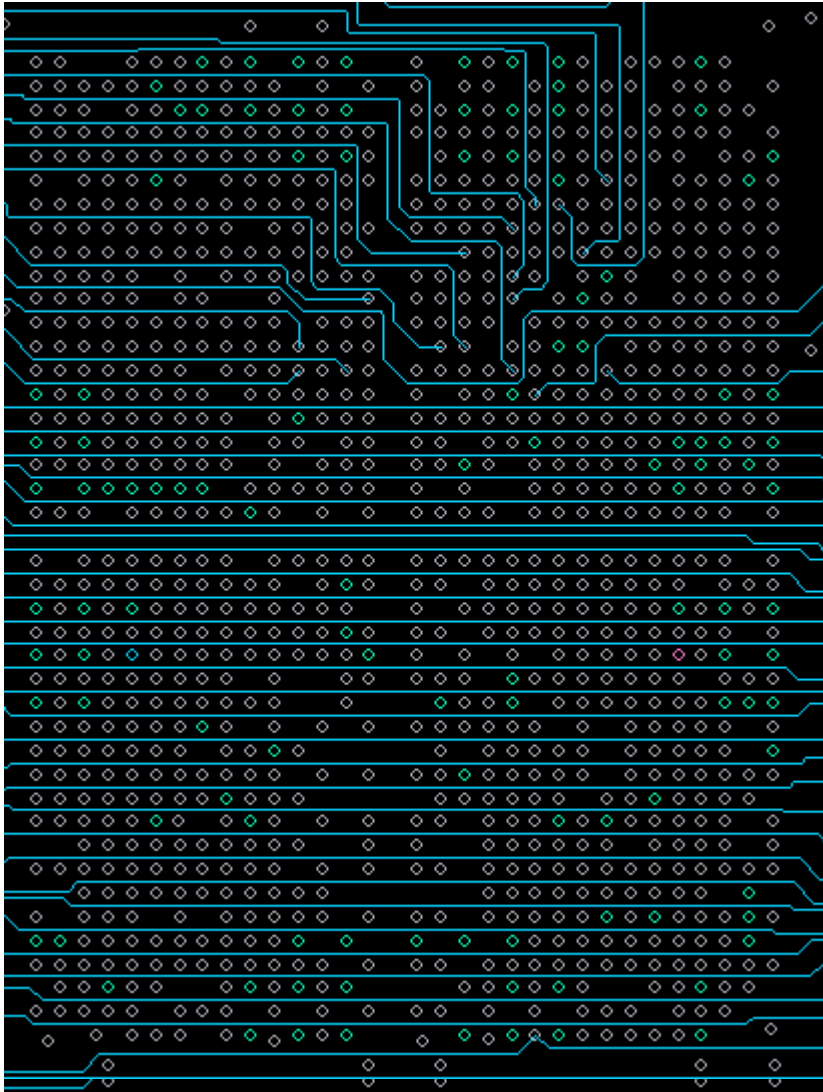
*CopperCAD*<sup>TM</sup>

**CADWare**

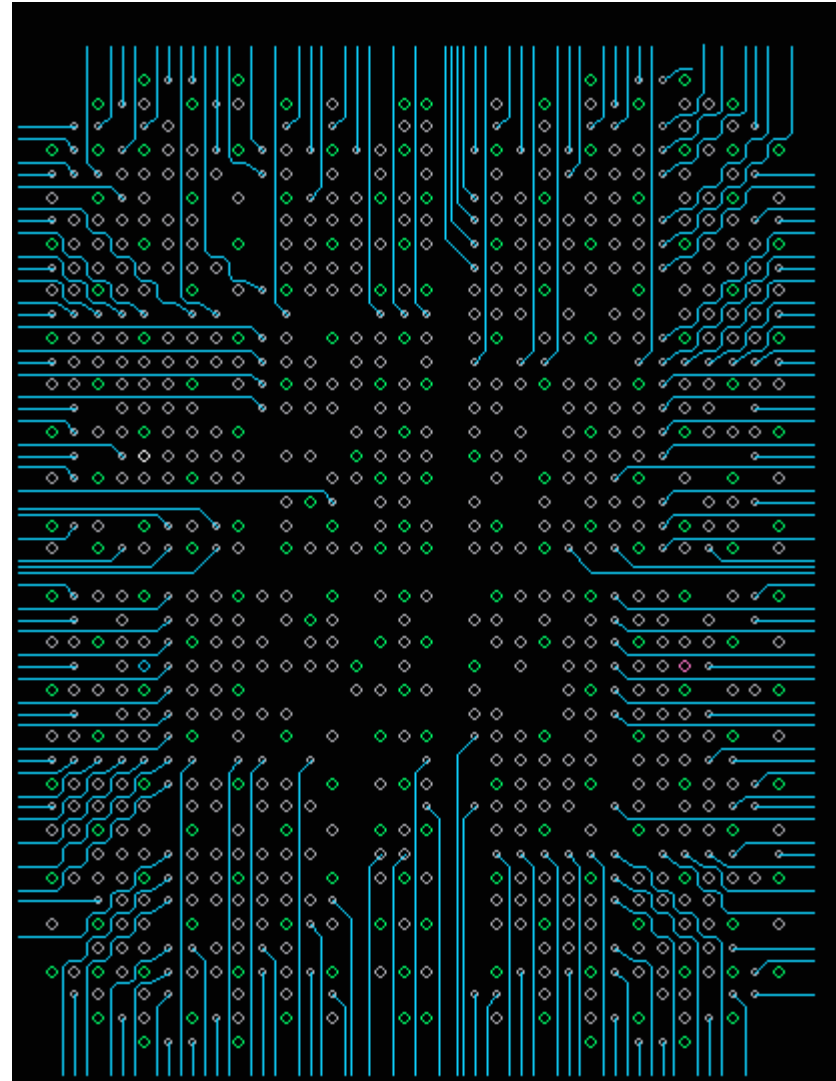
[www.coppercad.com](http://www.coppercad.com)

# BGA 1247

Original Routing – Layer 1

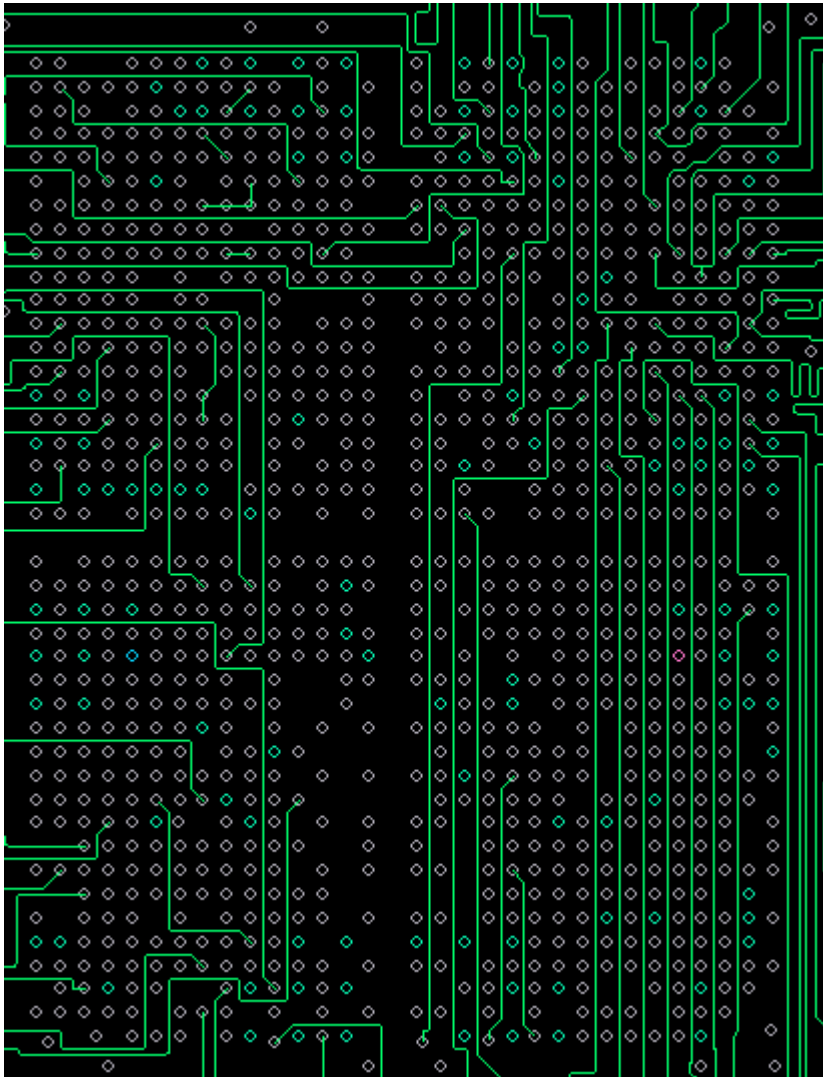


Channel Routing – Layer 1

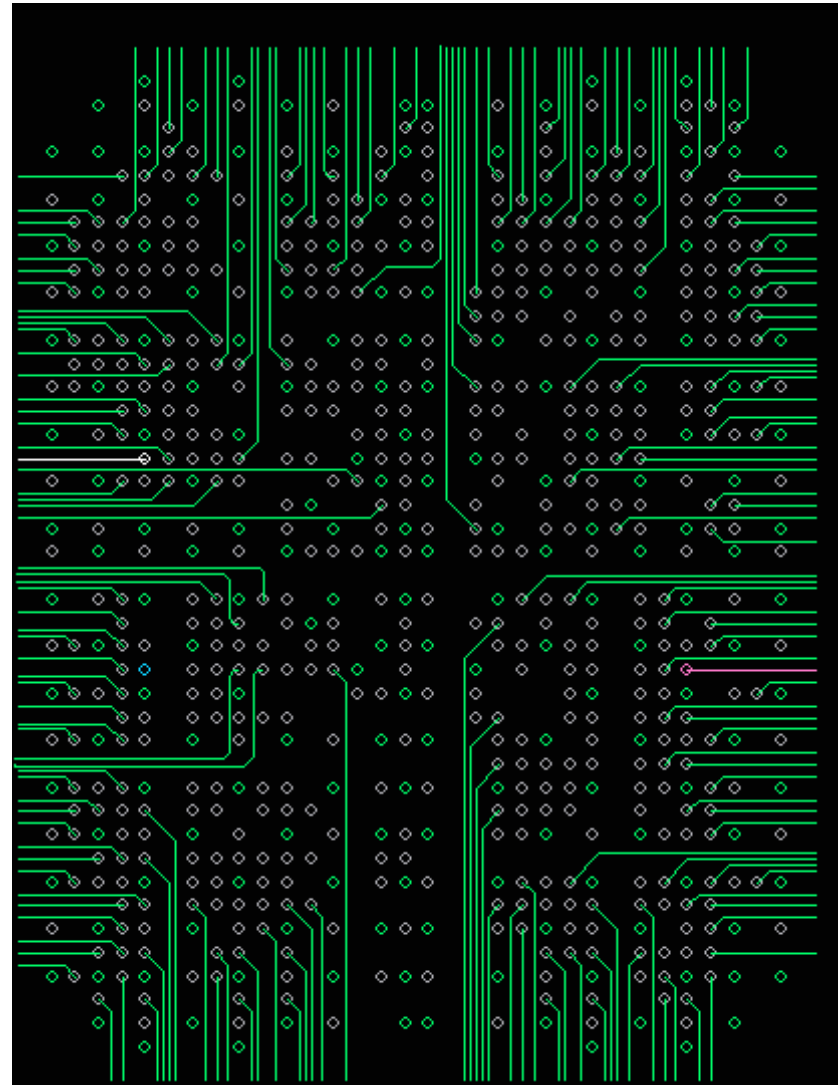


# Signal Layer 2

Original Layer 2

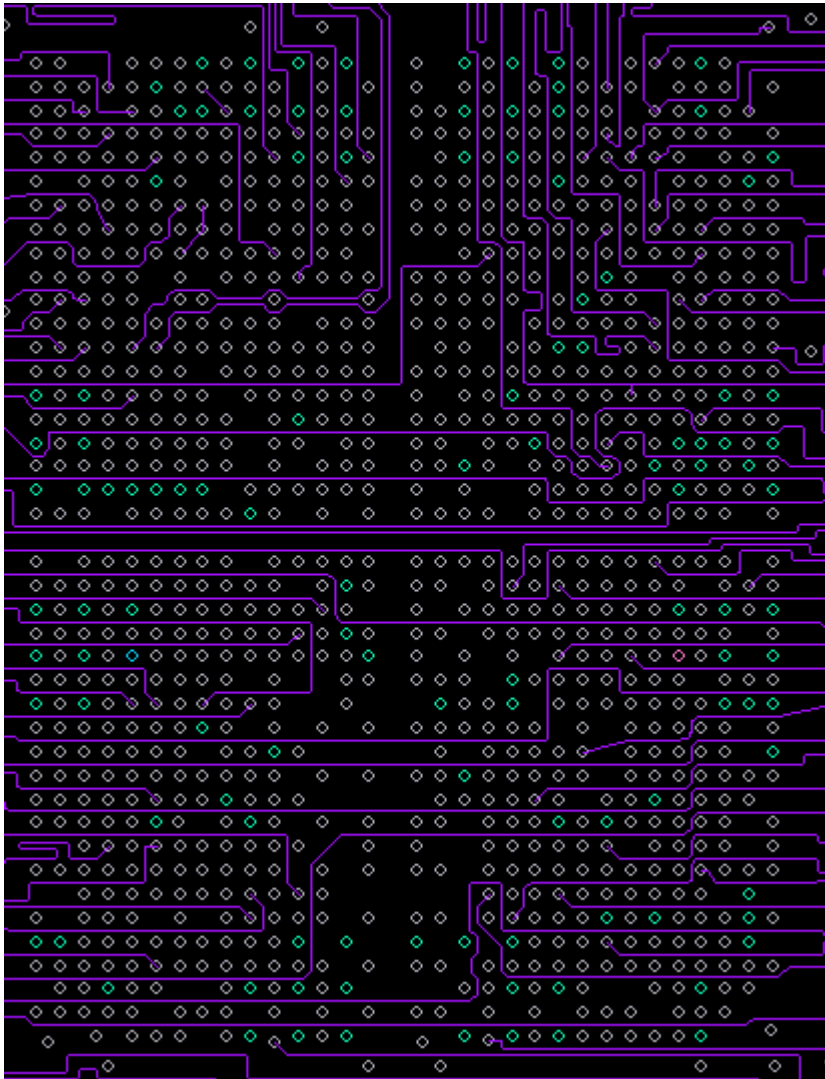


Channel Routing

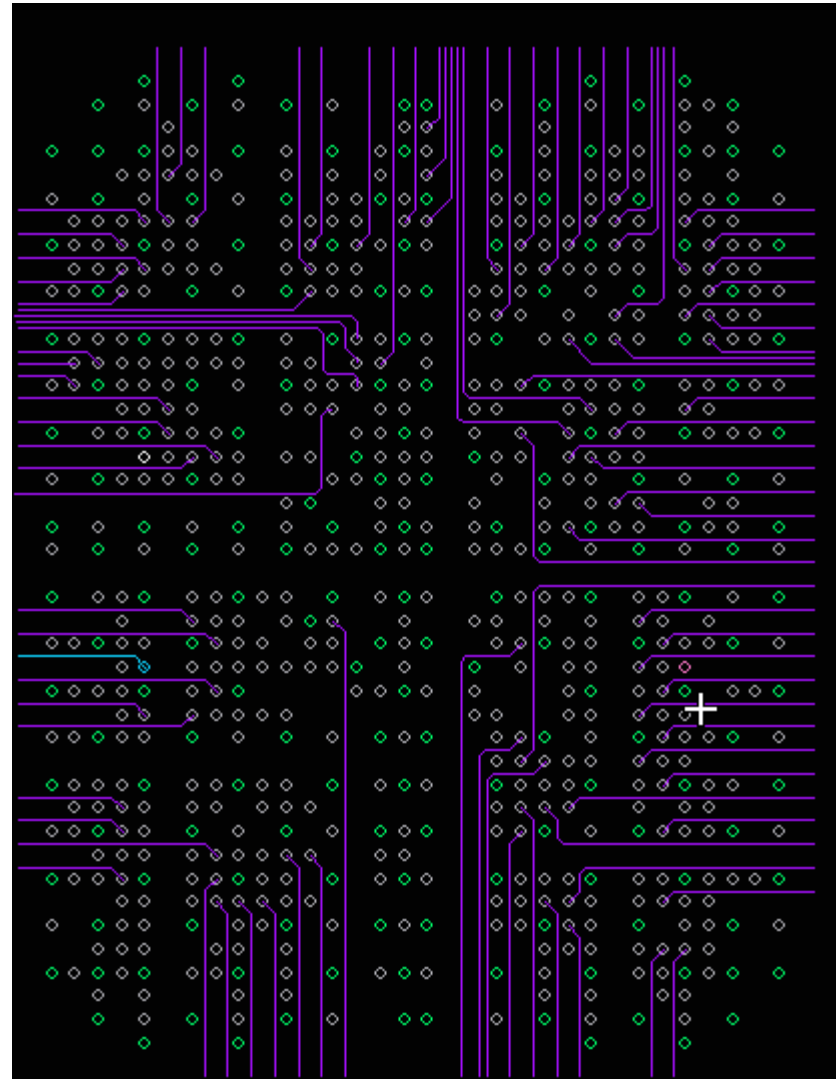


# Signal Layer 3

Original Layer 3

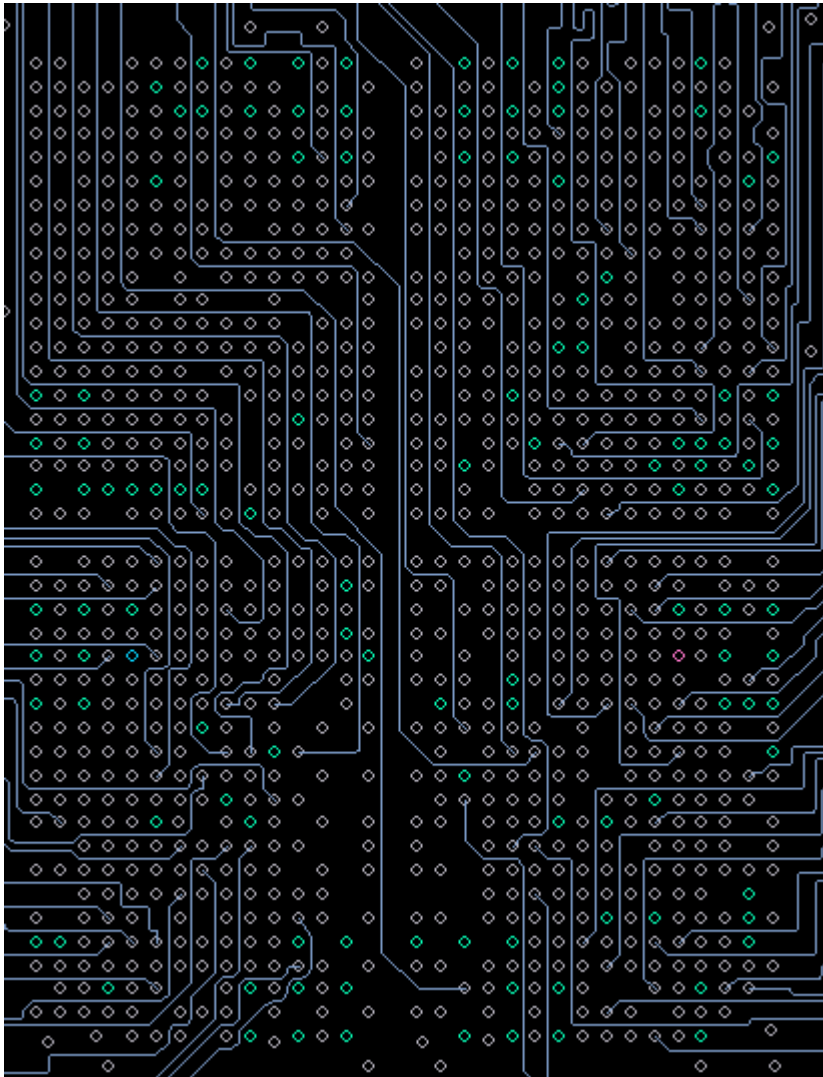


Channel Routing

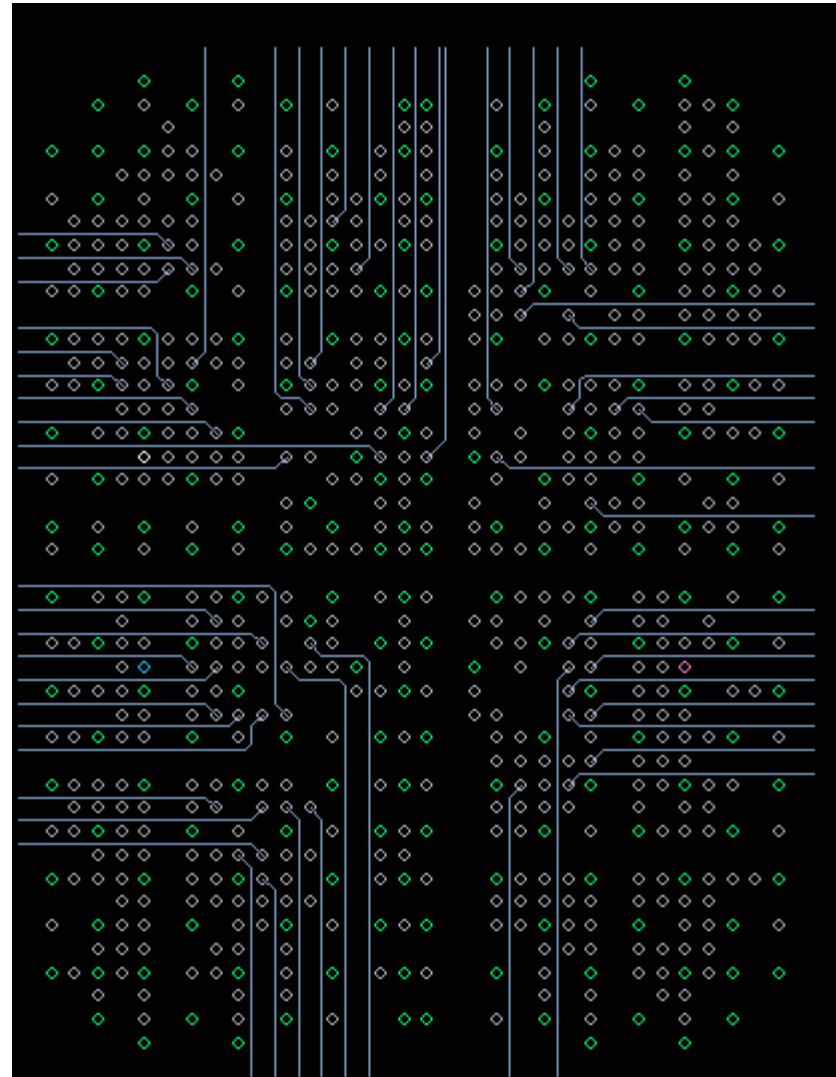


# Signal Layer 4

Original Layer 4

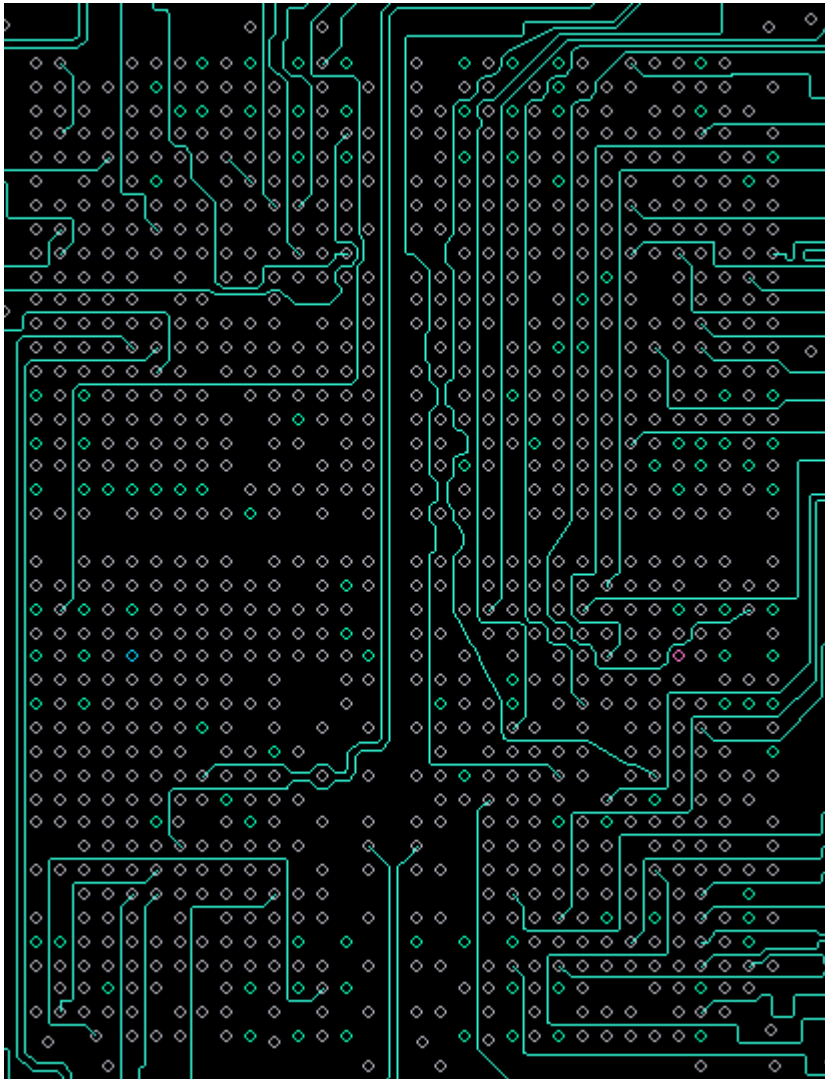


Channel Routing

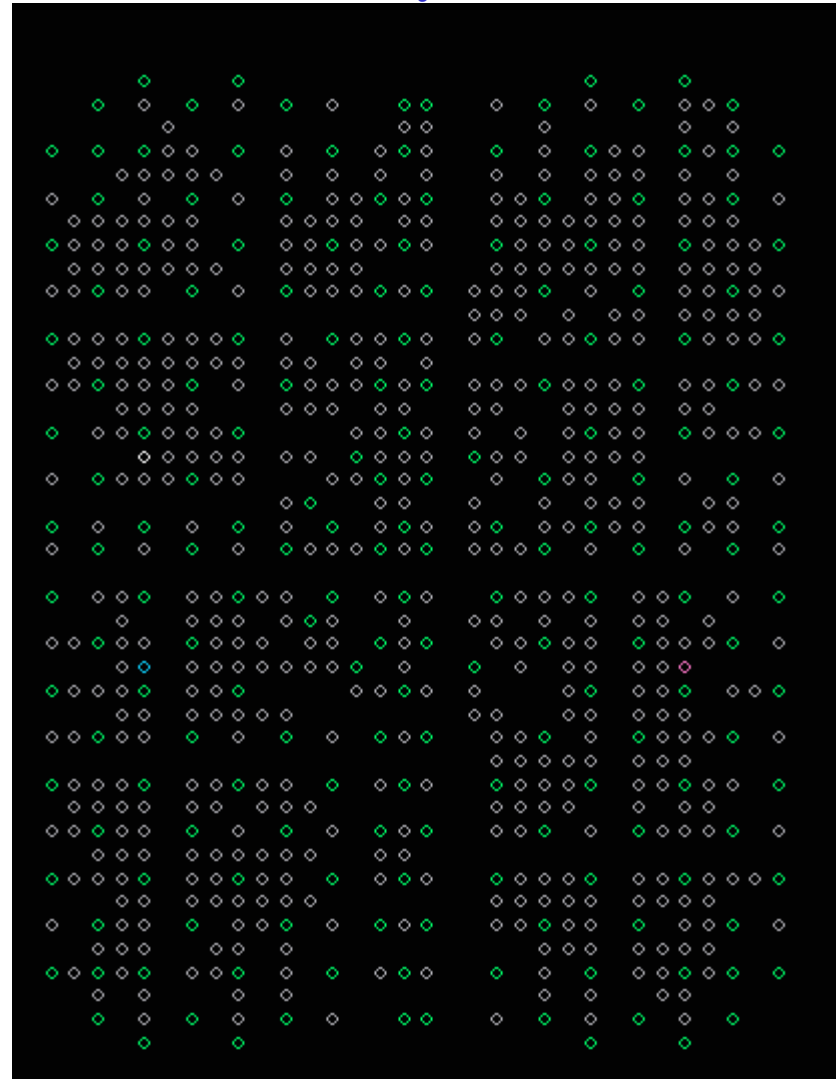


# Signal Layer 5

Original Layer 5

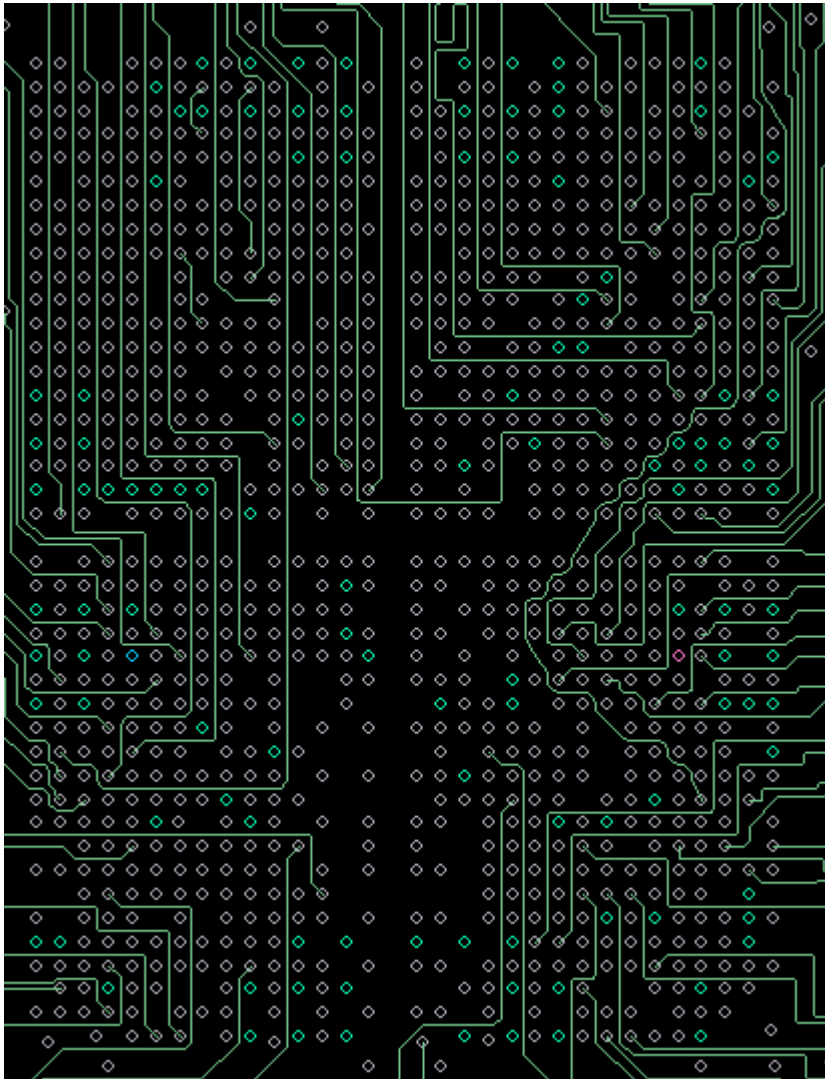


Channel Routing --- empty layer  
**First Layer Saved**

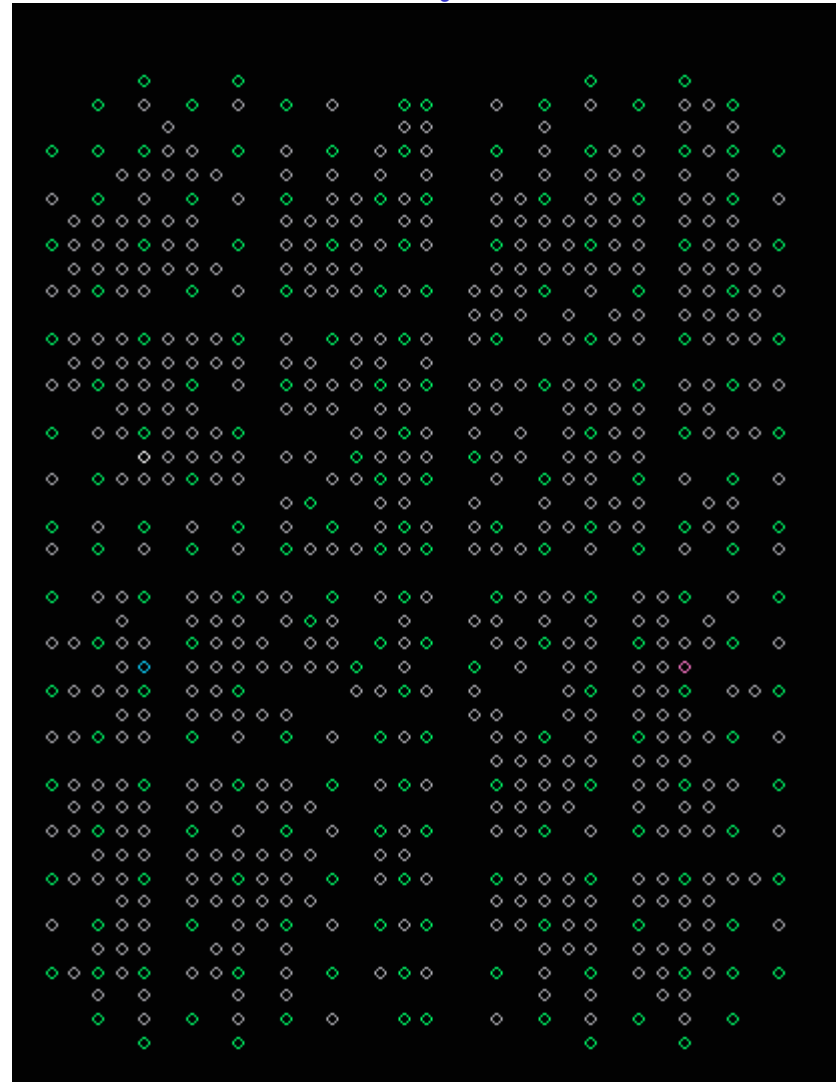


# Signal Layer 6

Original Layer 6

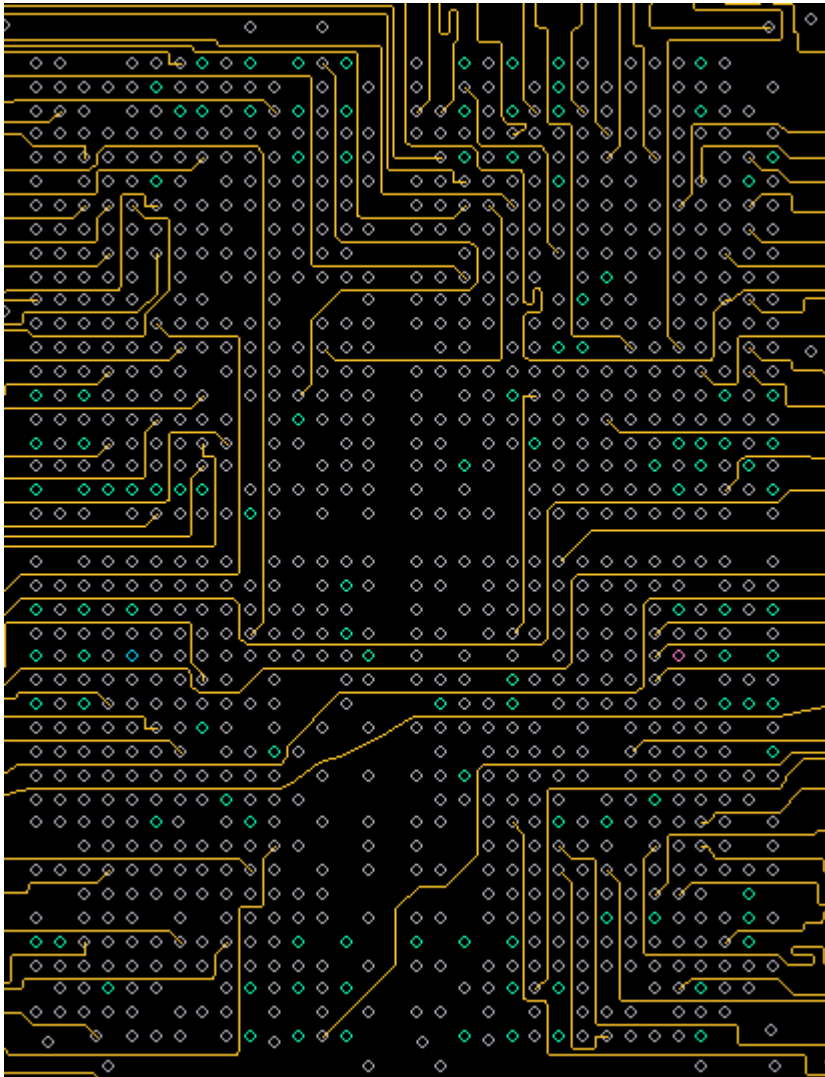


Channel Routing --- empty layer  
**Second Layer Saved**

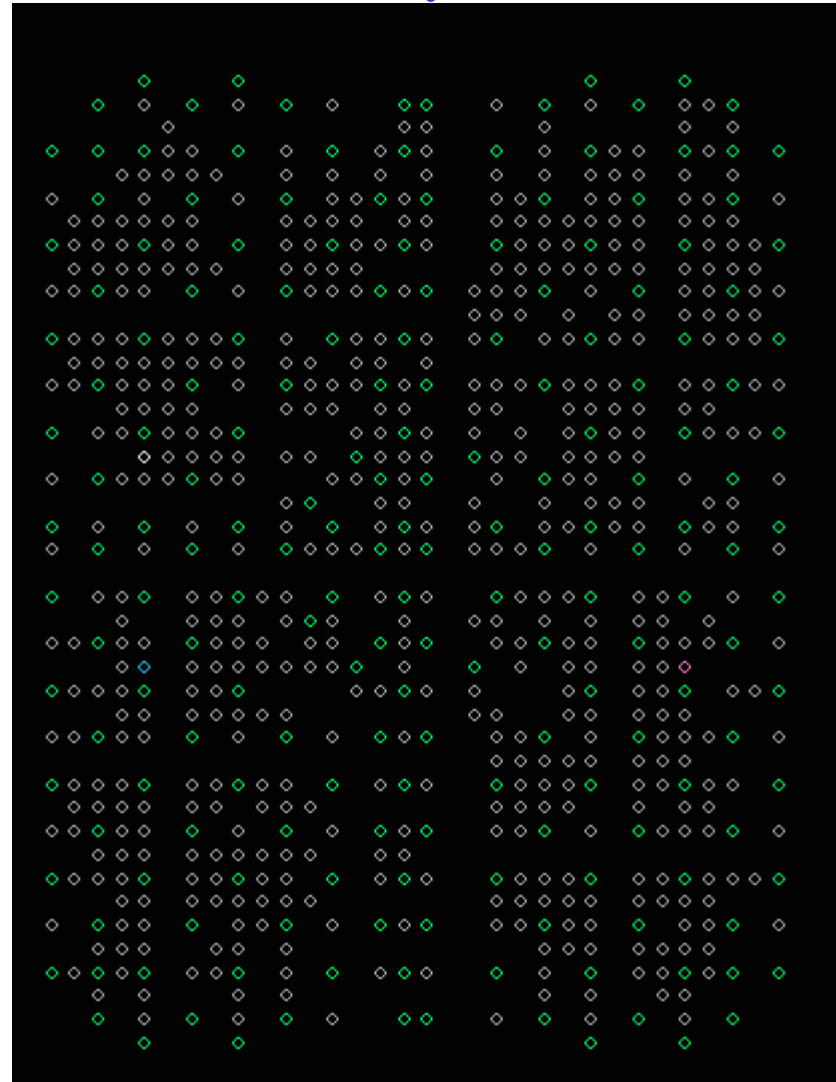


# Signal Layer 7

Original Layer 7

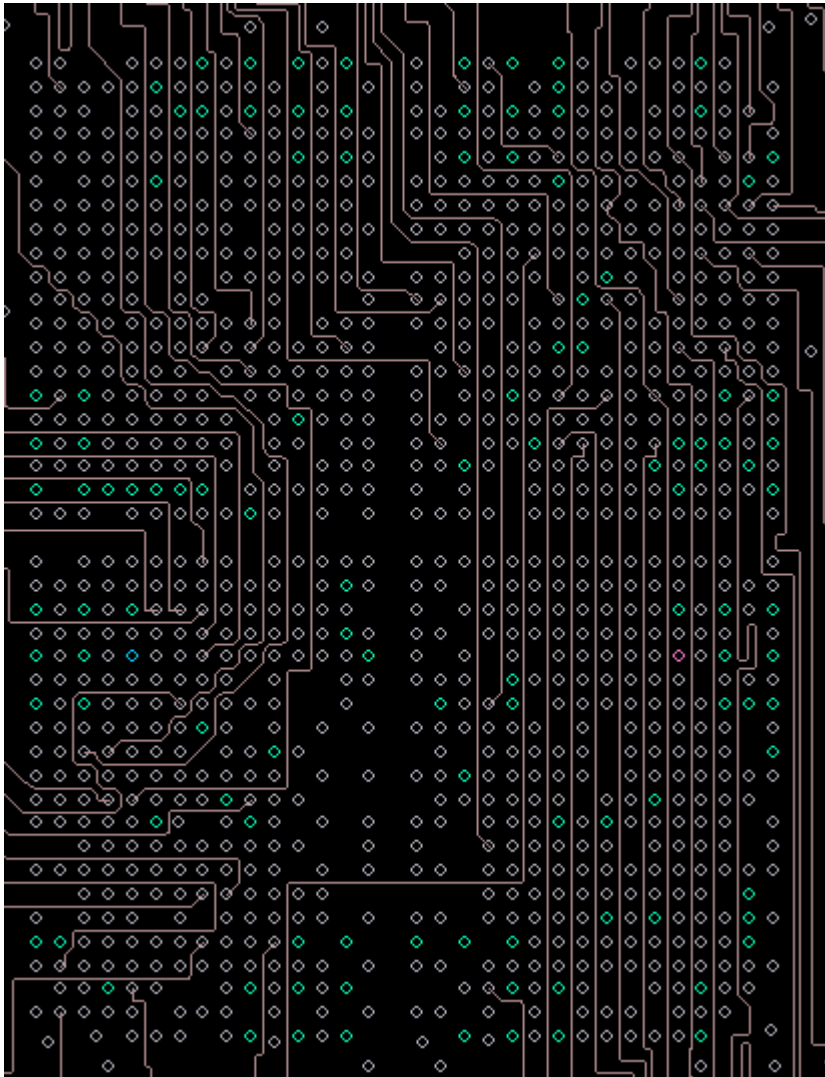


Channel Routing --- empty layer  
**Third Layer Saved**

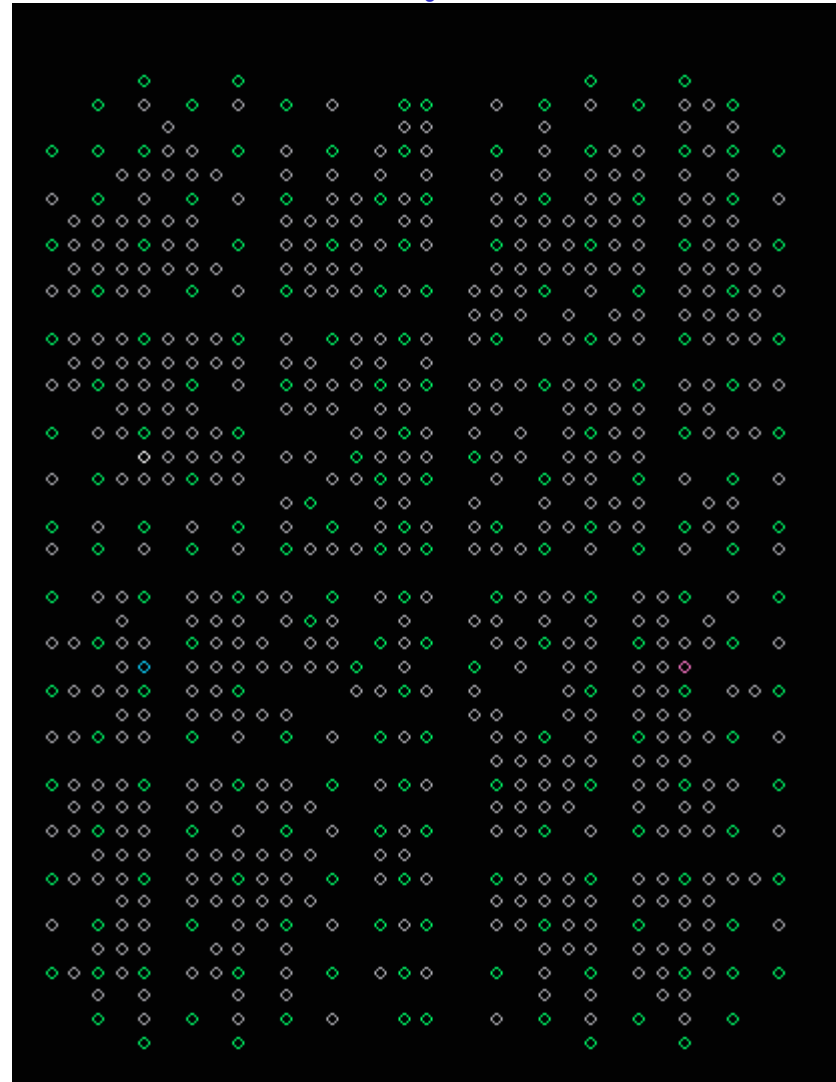


# Signal Layer 8

Original Layer 8

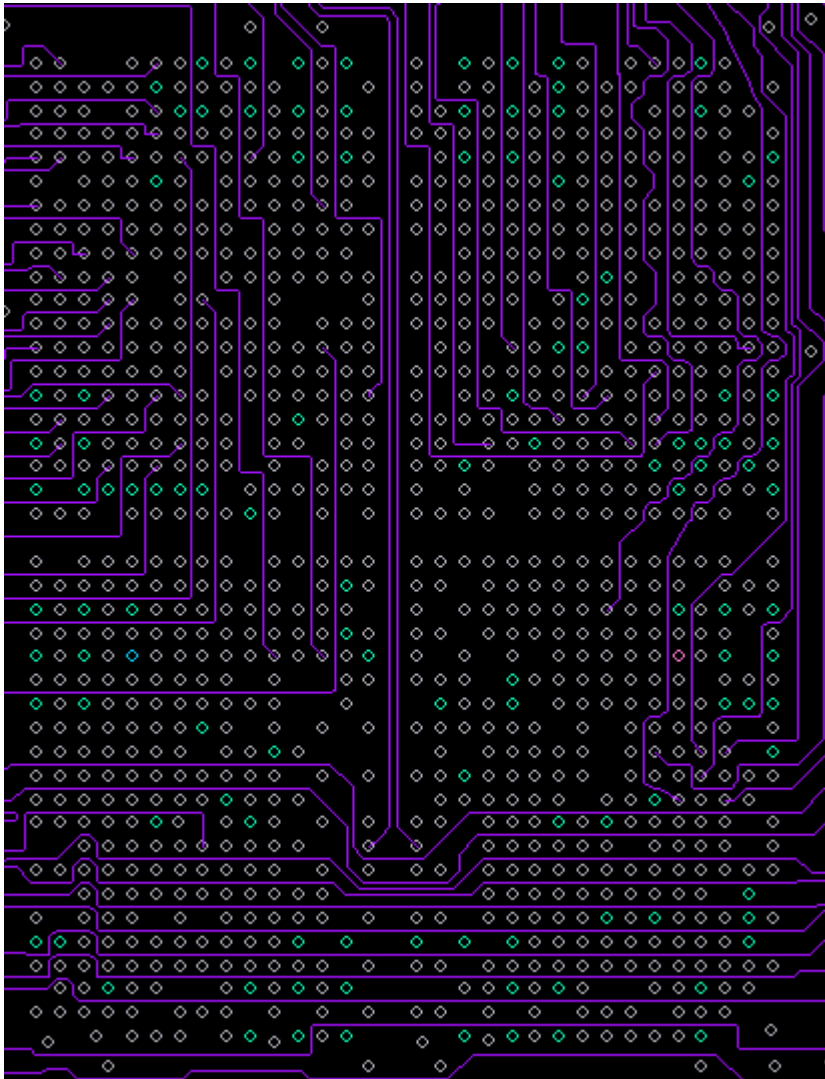


Channel Routing --- empty layer  
**Forth Layer Saved**

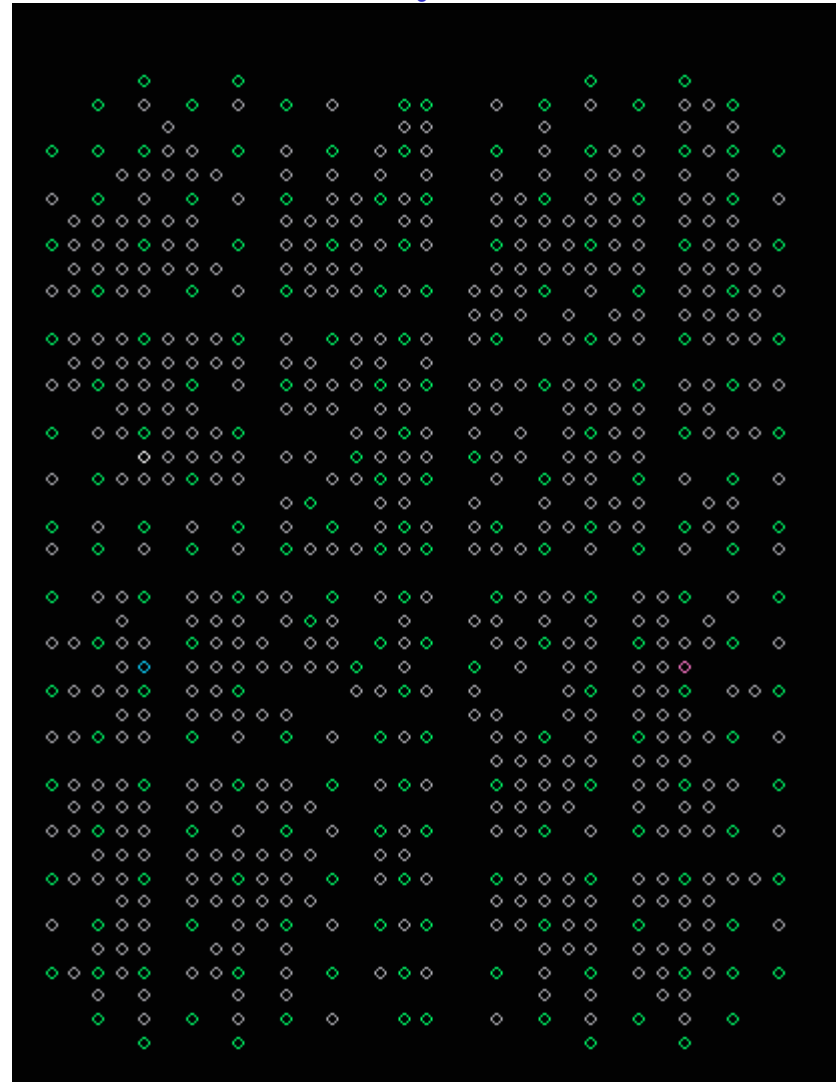


# Signal Layer 9

Original Layer 9



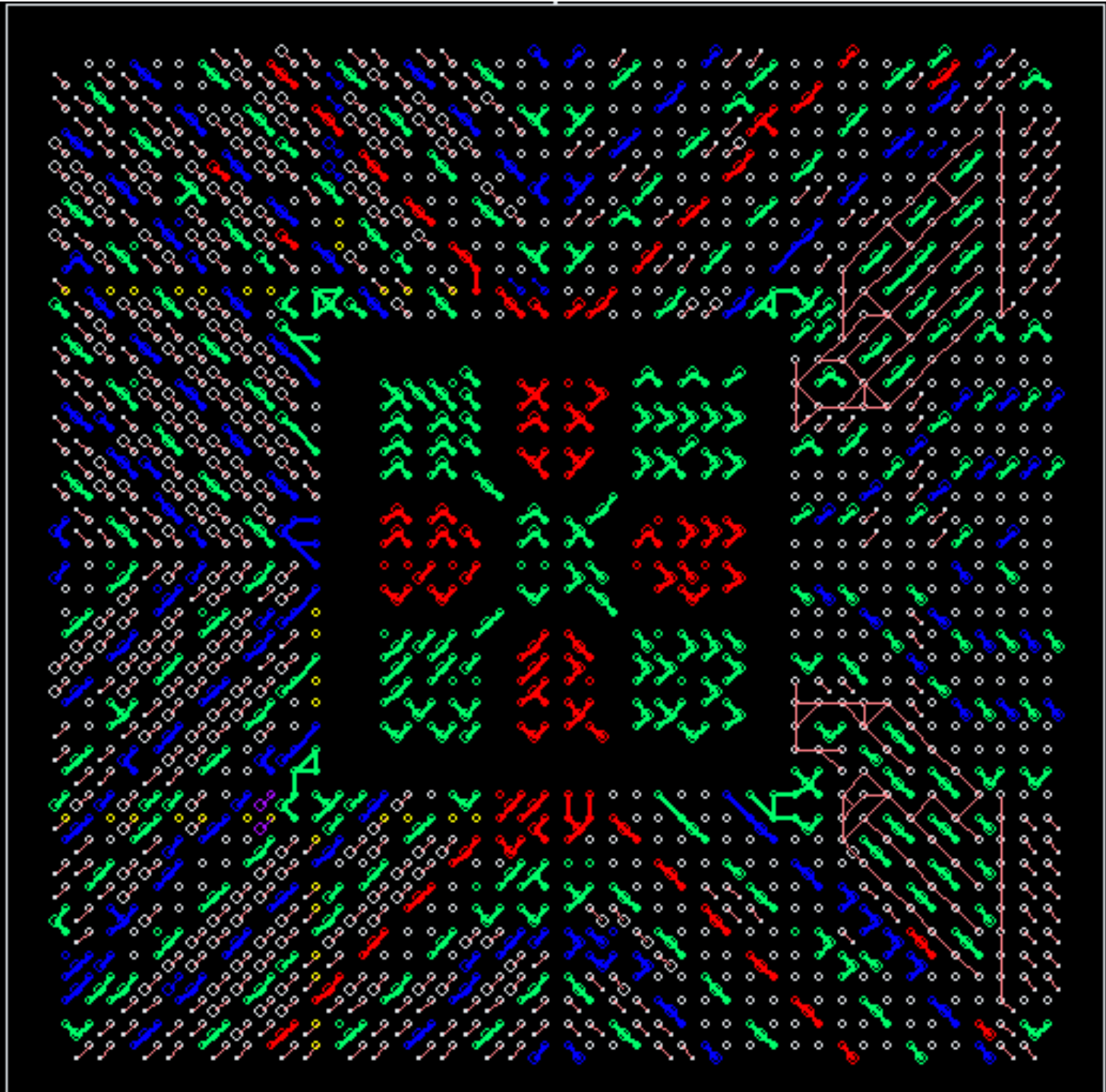
Channel Routing --- empty layer  
**Fifth Layer Saved**



# Channel Routing

Example of a 1724 pin BGA with a large number of power and same net logic pins that can share vias.

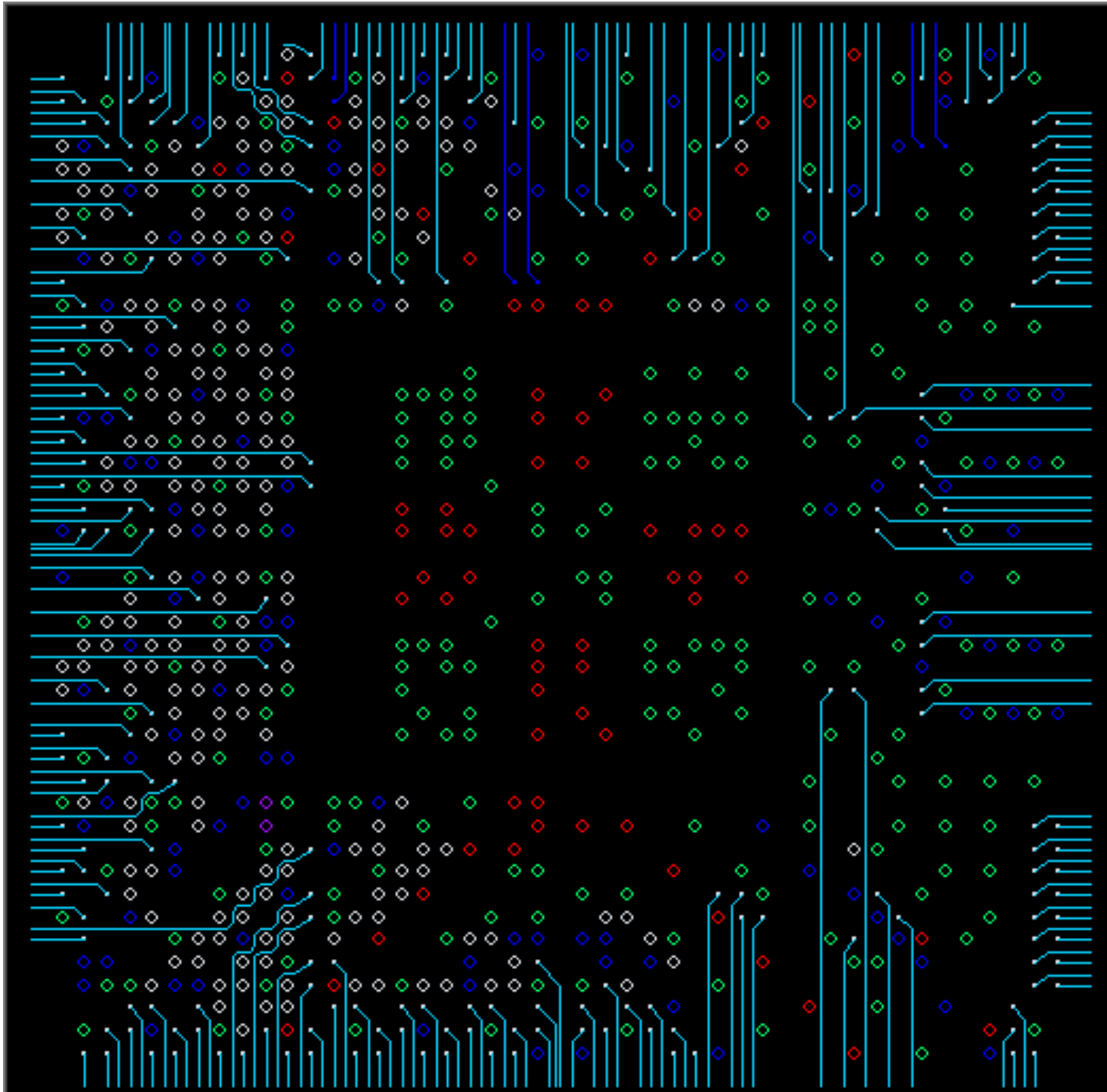




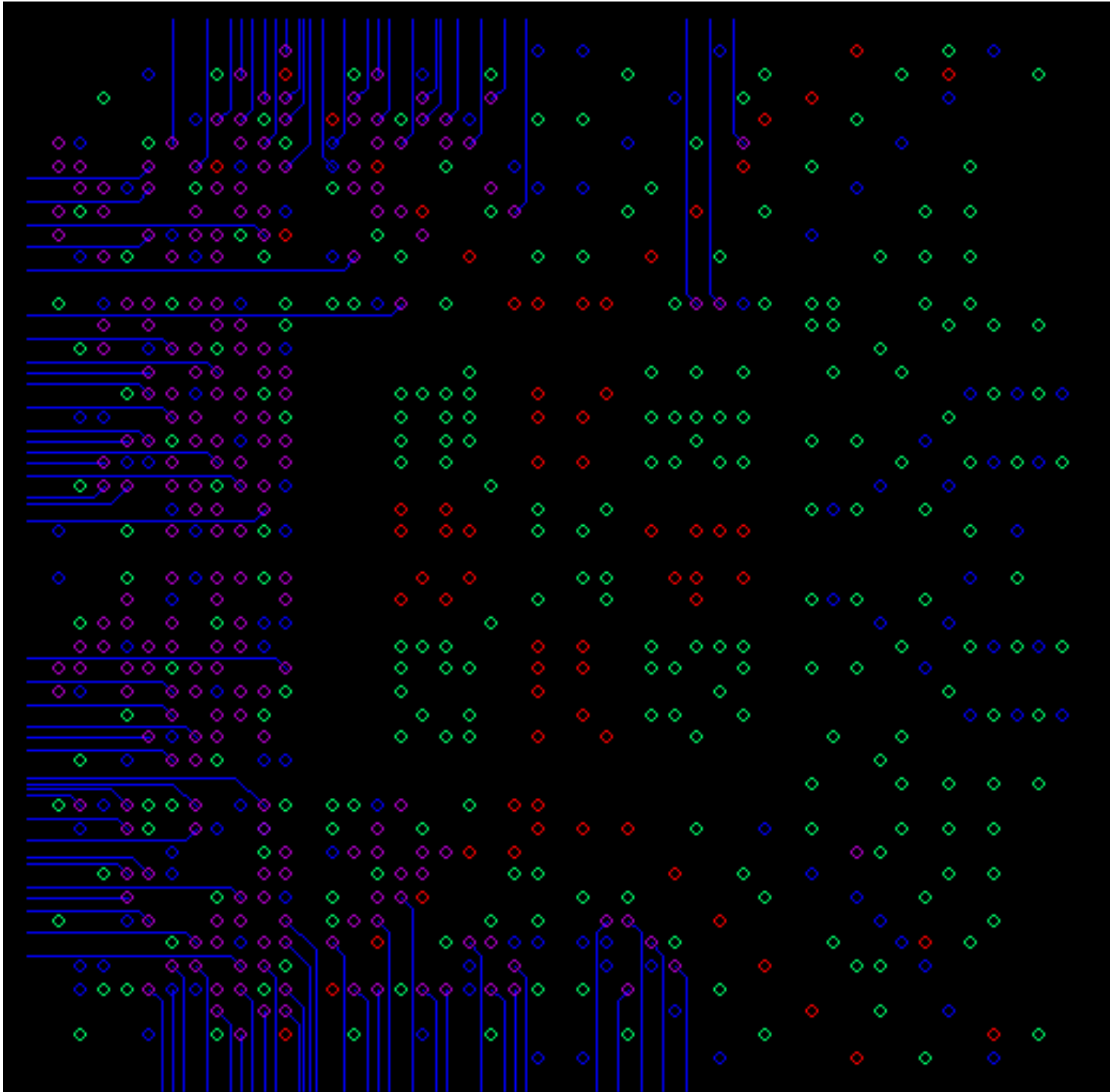
44 x 44 Pins,  
minus 212  
missing pins =  
1724 remaining  
pins

If power and  
logic pins use  
the via sharing  
option....

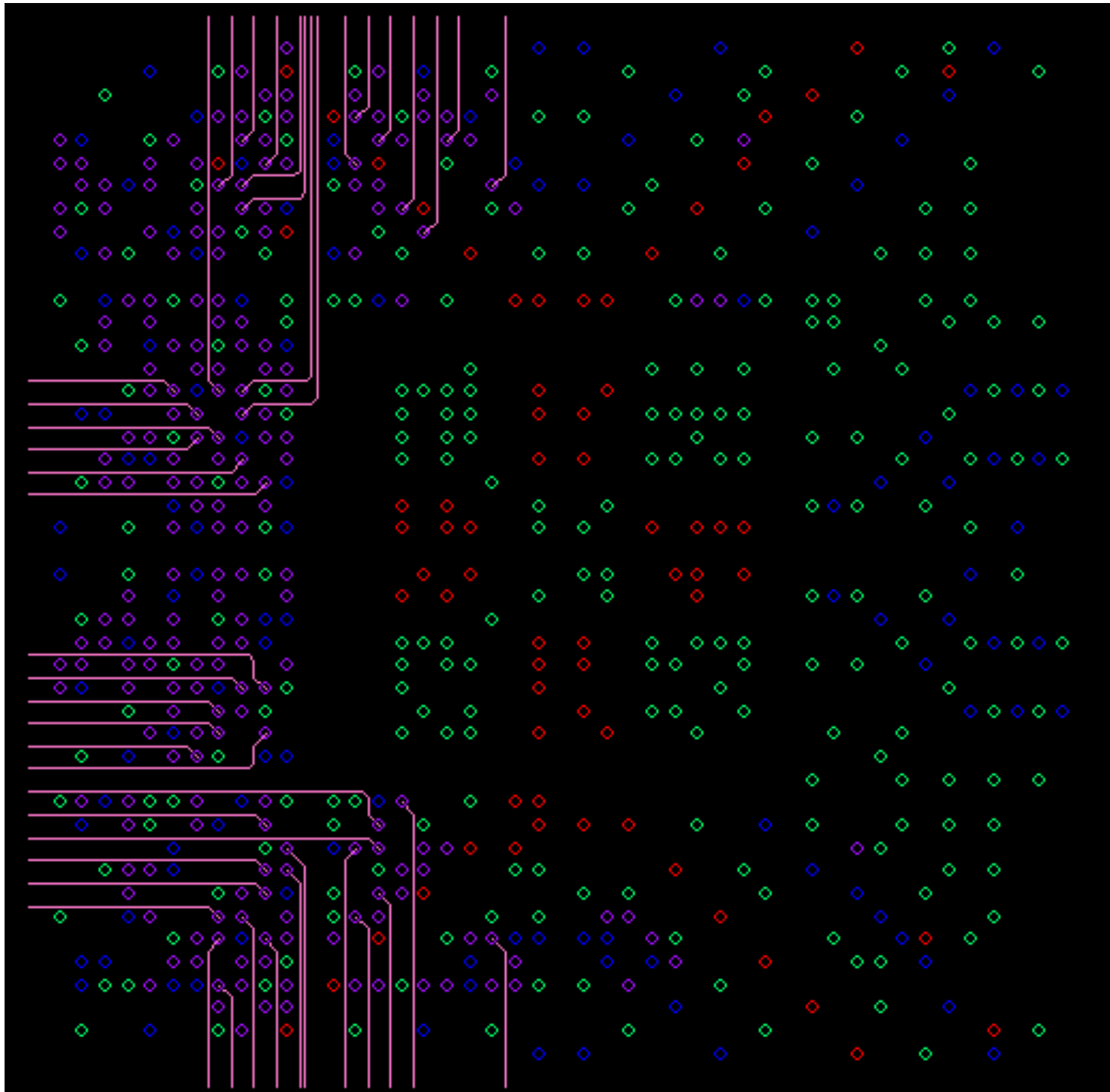
This BGA  
becomes very  
easy to route.



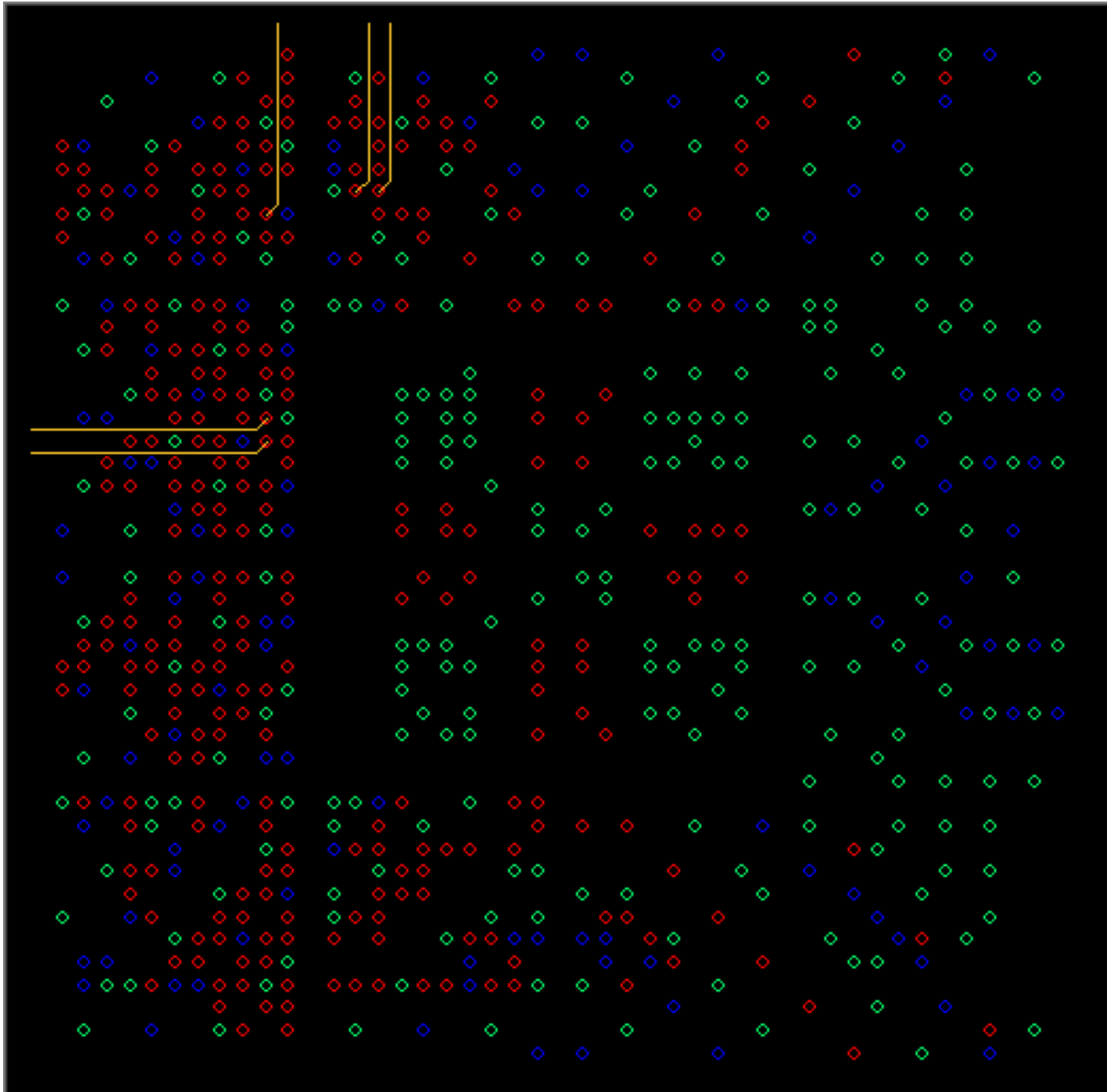
75 percent of the logic signals could be routed on the first inner layer.



The remainder of the signals are routed on the next two layers.

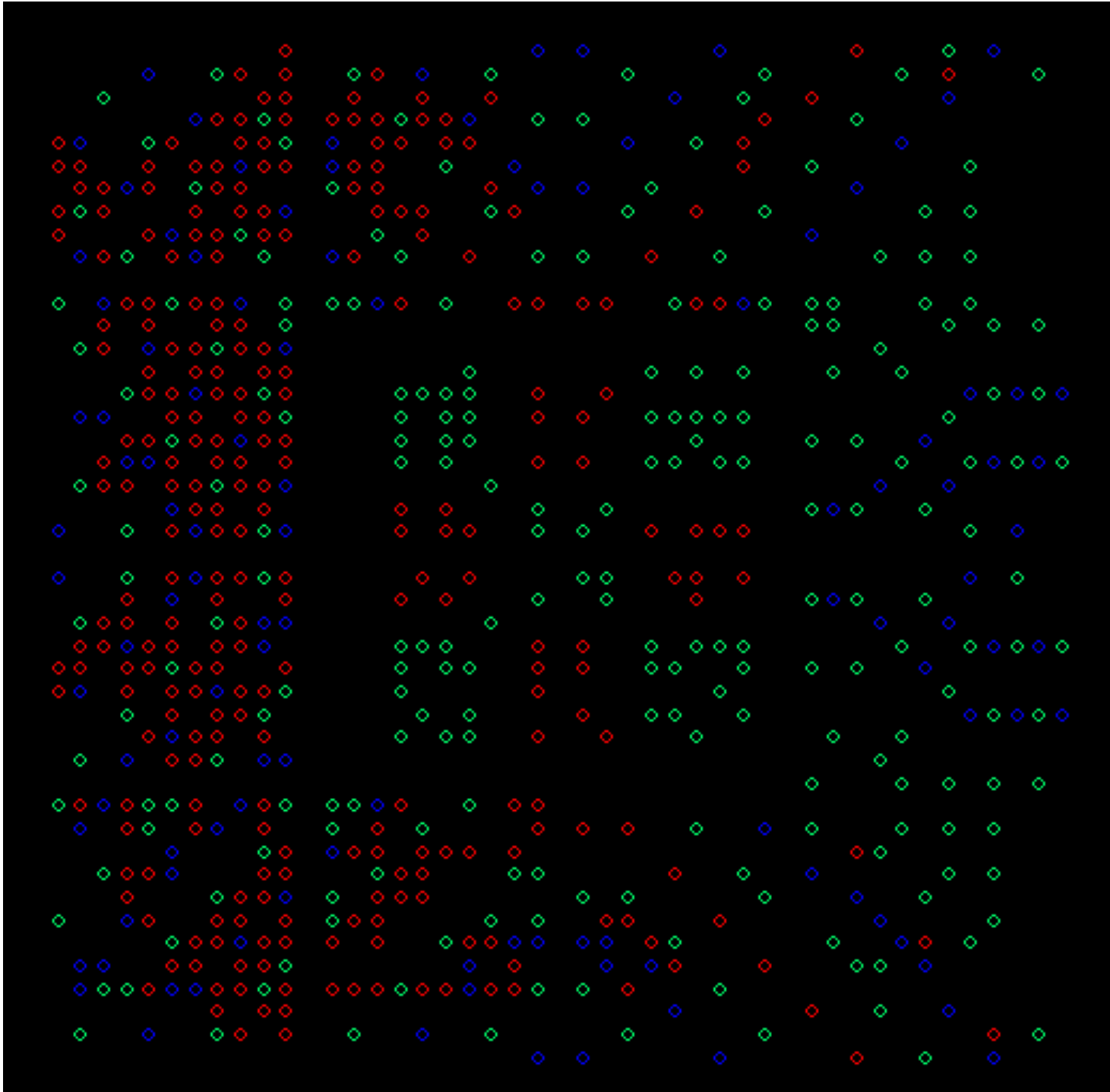


99 percent of the logic signals are routed by the end of the third layer.



The fourth layer has only five logic signals to route.

However these could easily be cleaned up and routed on previous layers.



Any other layers under the BGA are now open to allow routing from the rest of the board to pass through.

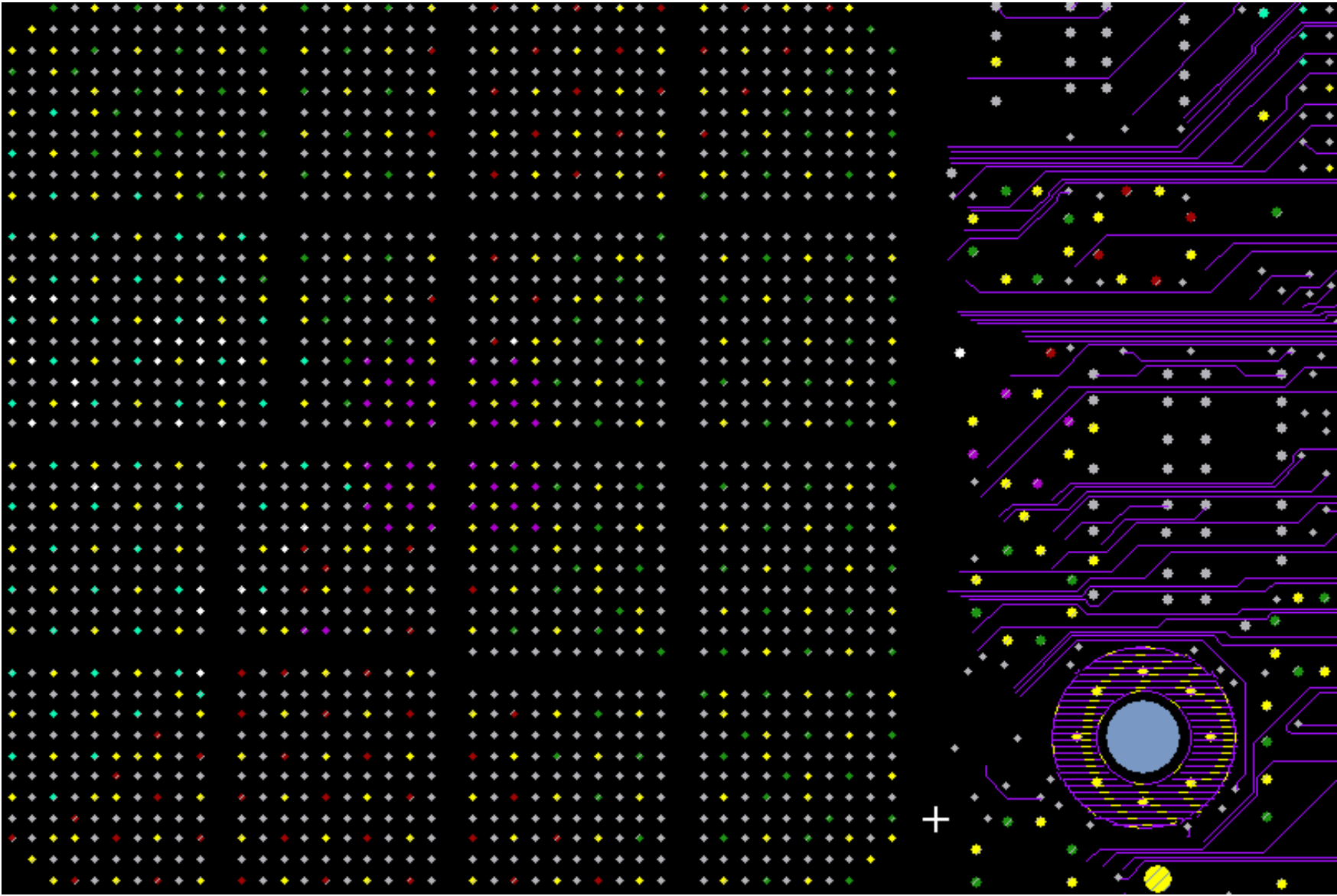
Chip capacitors also have many more placement locations under the BGA.

# Channel Routing

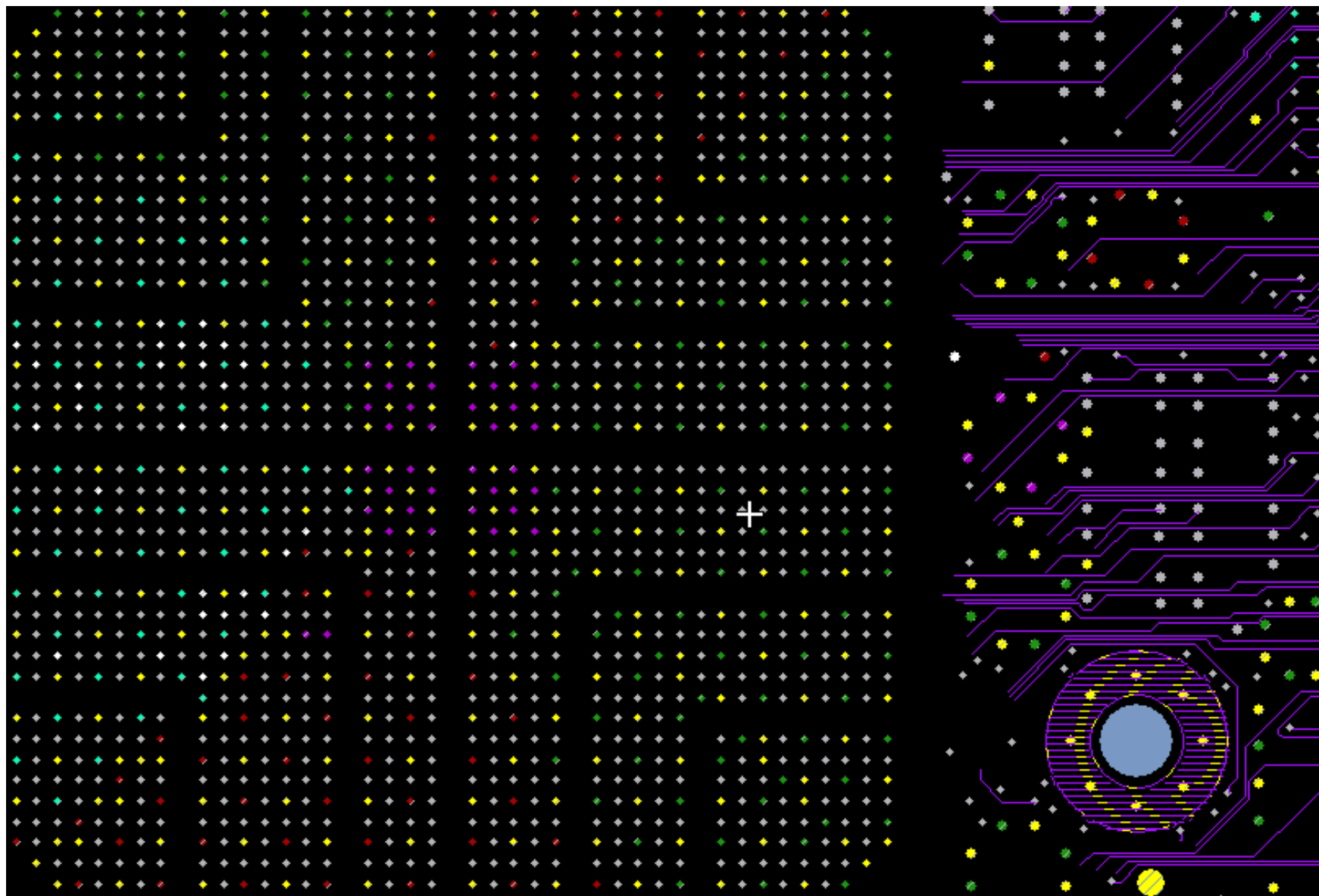
Available options for Channel creation Include  
BASIC CROSS AND “L” WITH EXTENTS



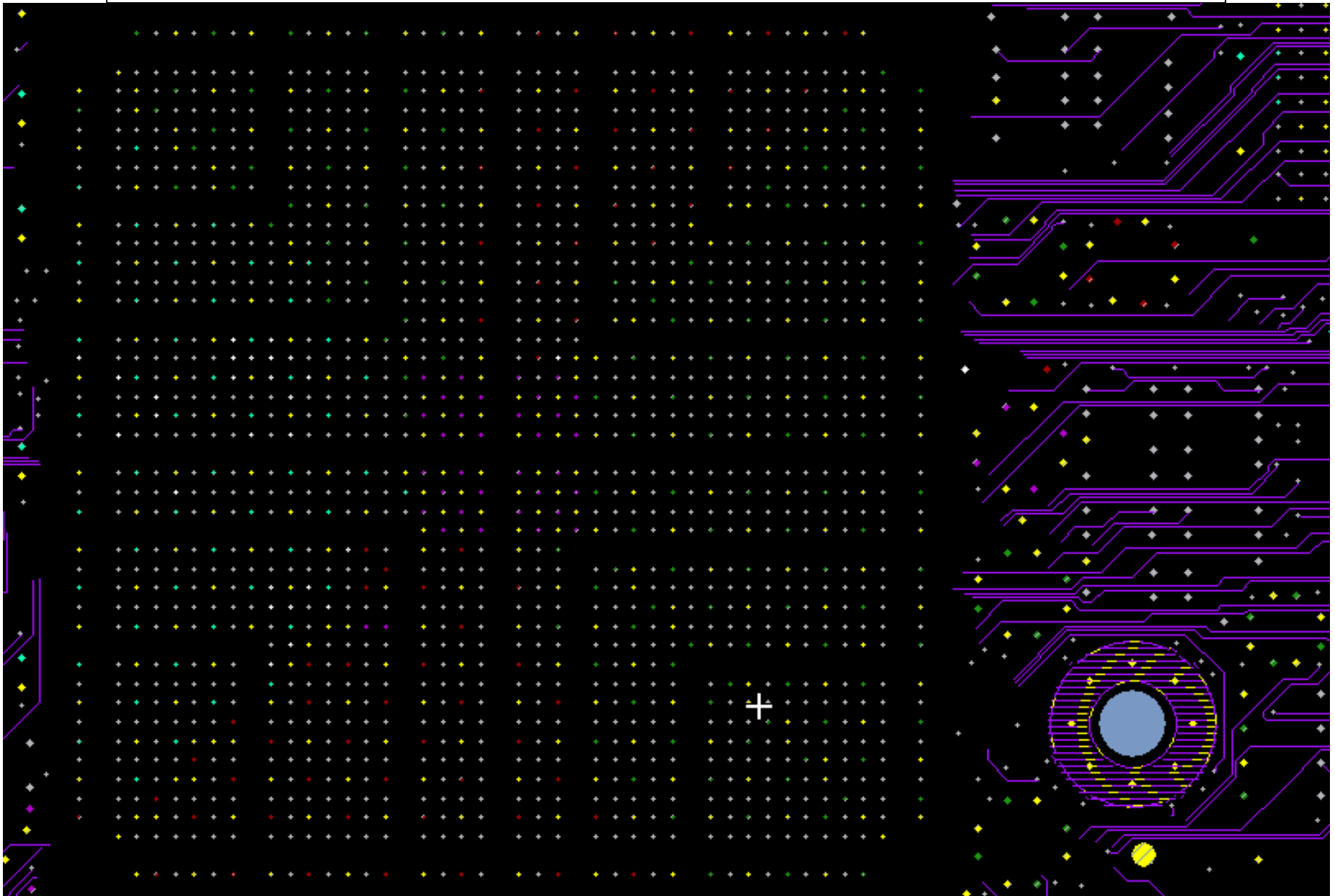
# BASIC CROSS ROUTING LAYER



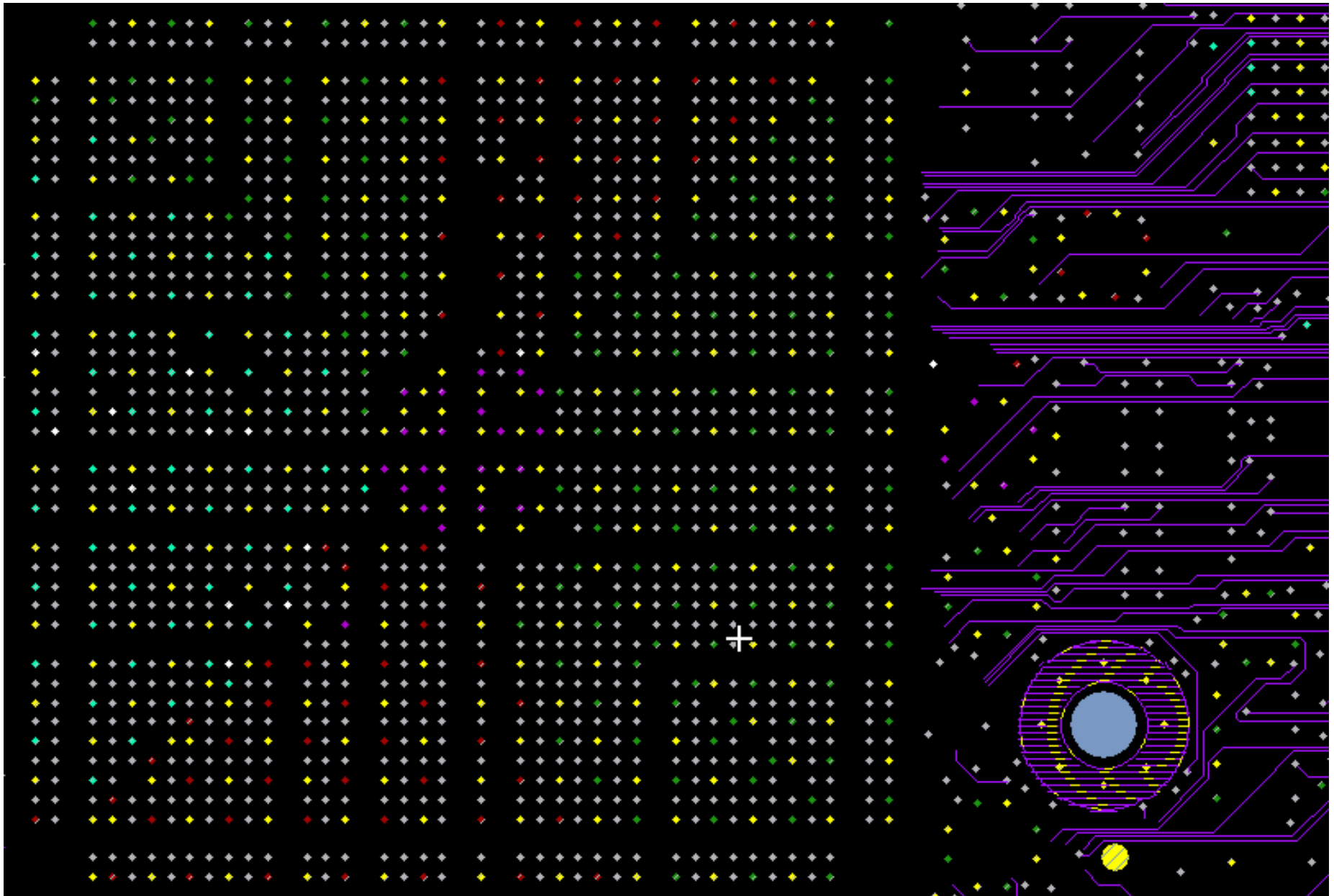
# BASIC “L” ROUTING LAYER



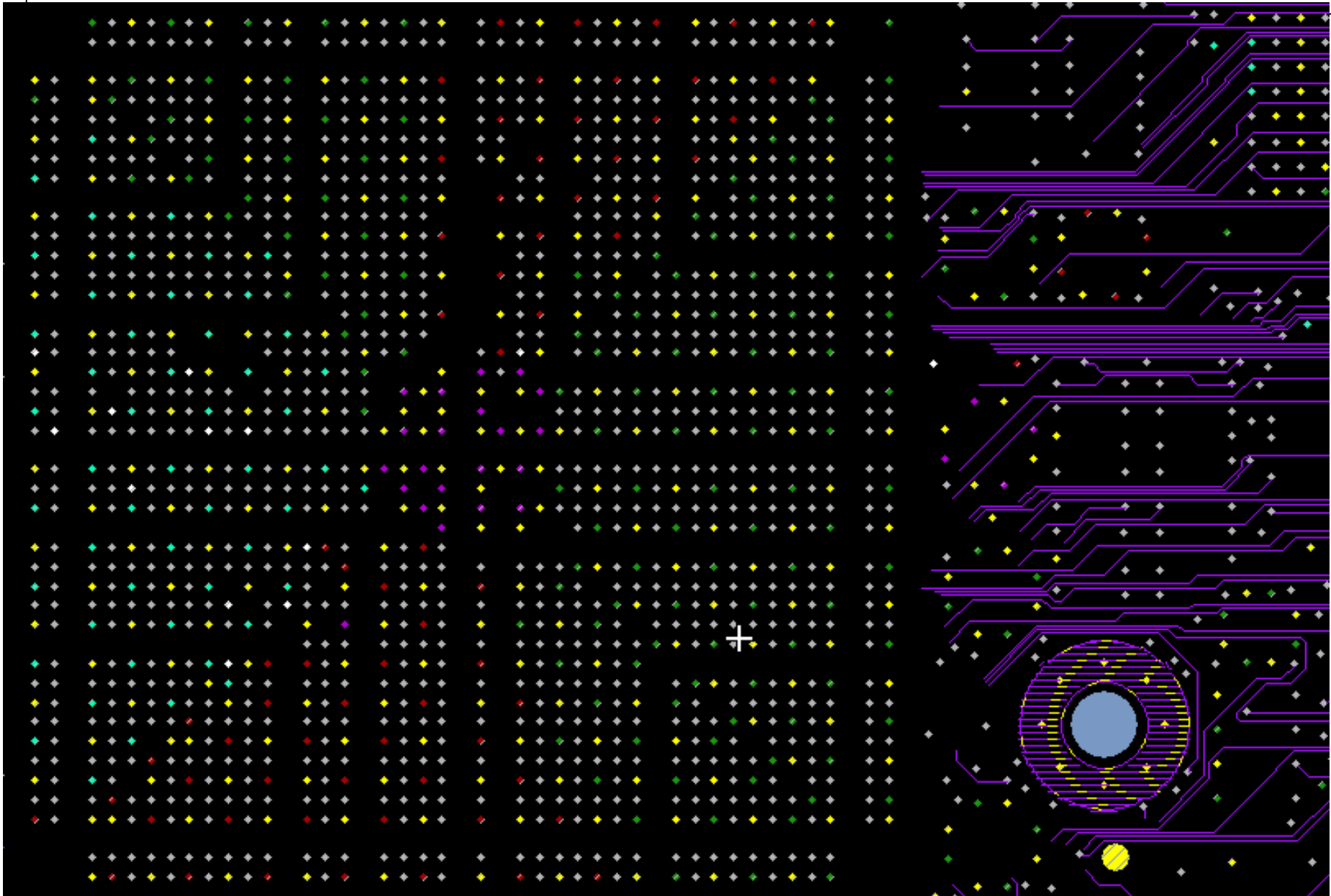
# 1 ROW EXTENT "L" ROUTING LAYER



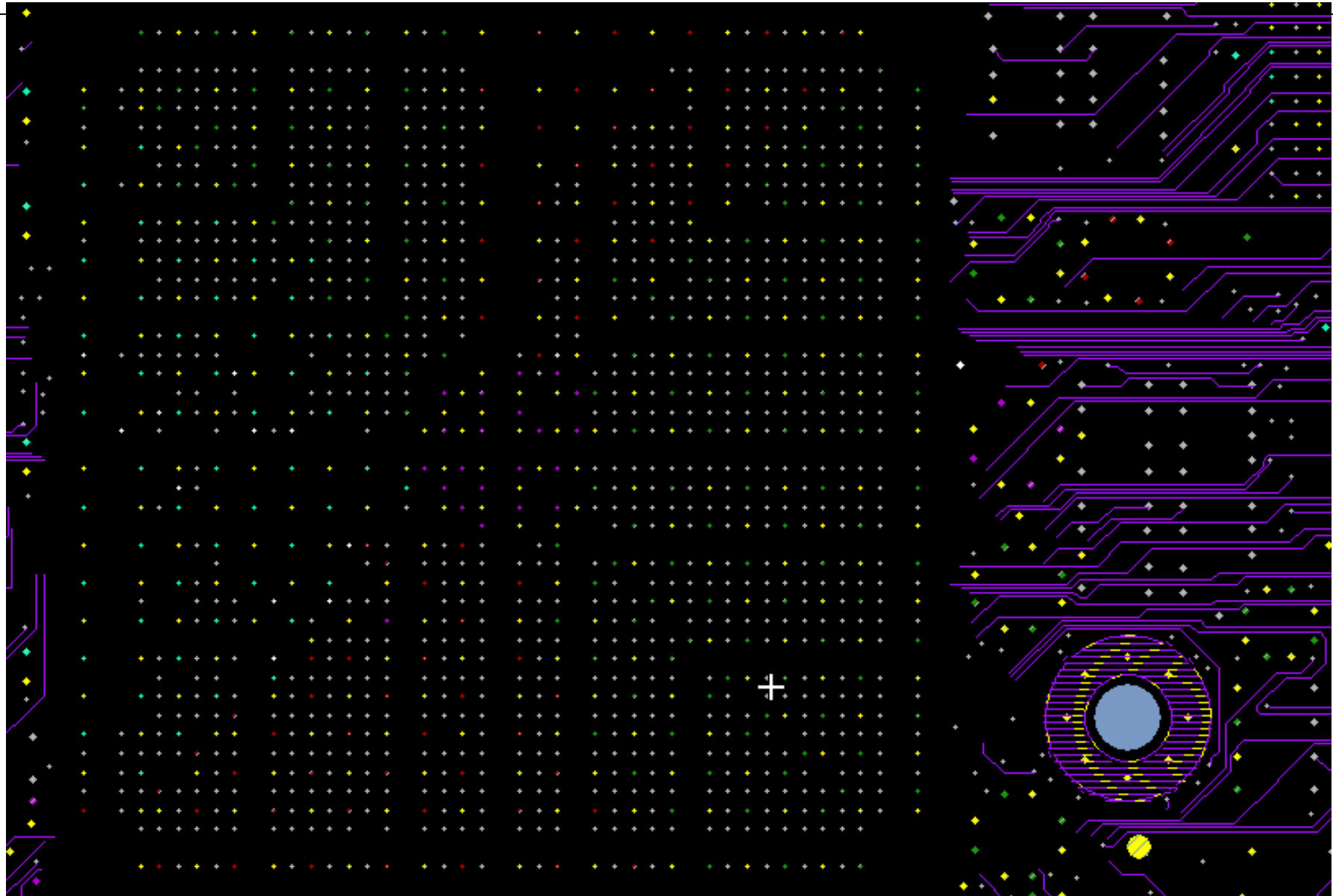
# 2 ROW EXTENT "L" ROUTING LAYER



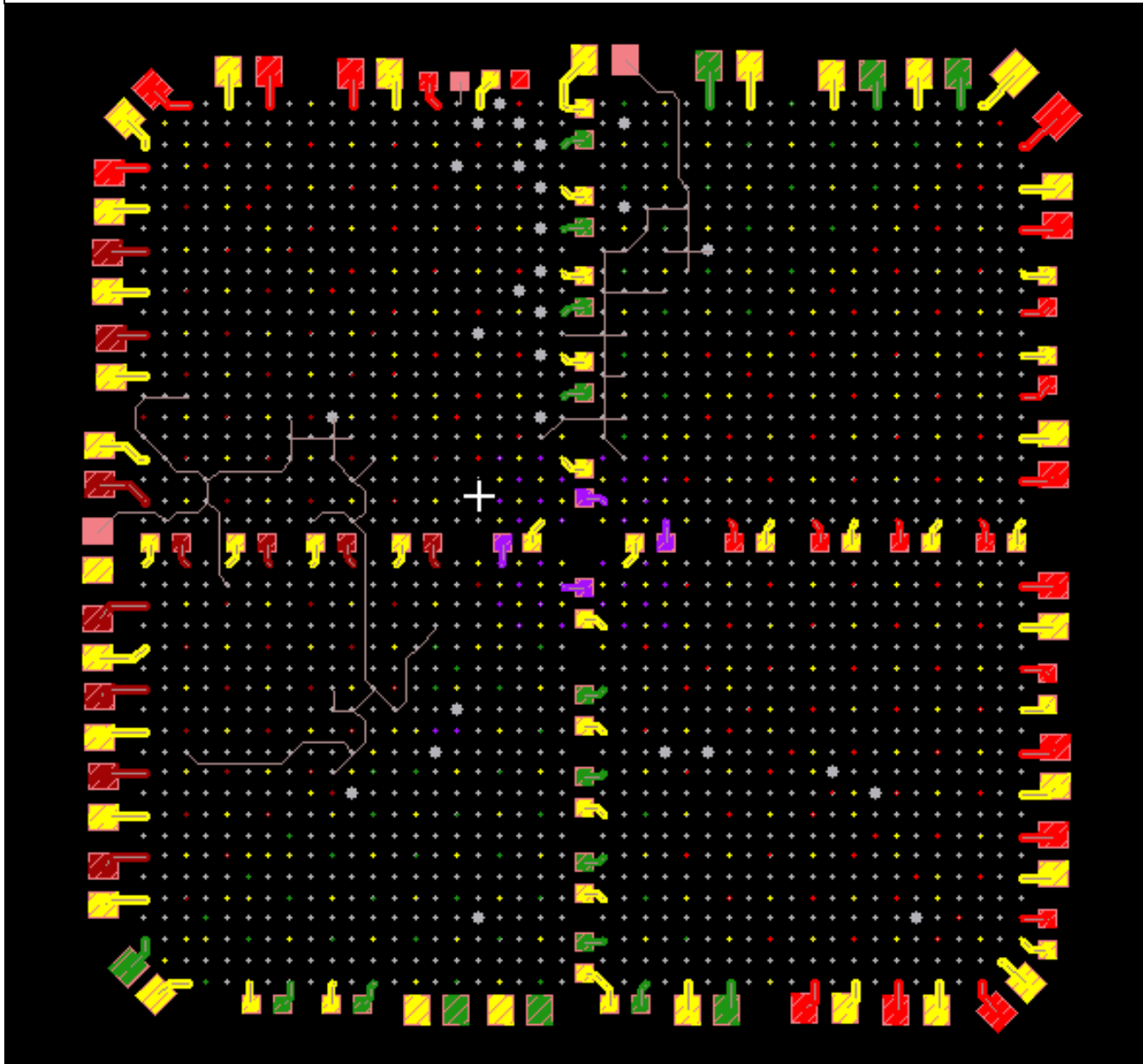
# 2 ROW EXTENT “L”, PWR & LOGIC SHARE ROUTING LAYER



# 1 ROW EXTENT “L”, PWR & LOGIC SHARE AND UNUSED NOT FANNED OUT

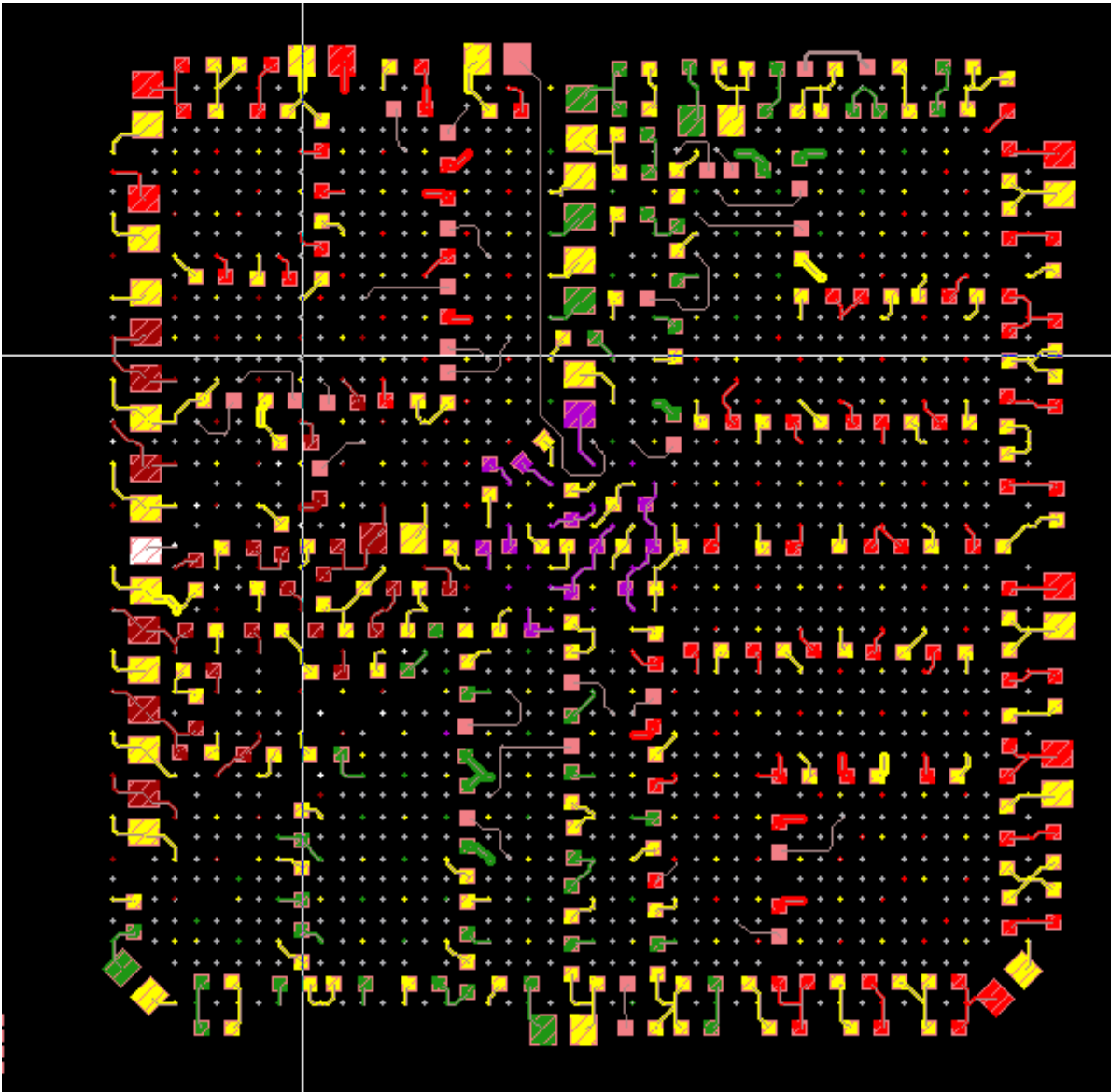


# REGULAR DISCRETE PLACEMENT



58 DISCRETES  
connected under  
the BGA  
sharing **116**  
VIAS.

# 1 ROW EXTENT “L”, PWR & LOGIC SHARE AND UNUSED NOT FANNED OUT BOTTOM



183 DISCRETES  
connected under  
the BGA sharing  
**366** VIAS  
compared to 116.

More than 3 times  
as much sharing