

# High Pin Count BGA routing Techniques

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# High Pin Count BGA routing Techniques



- **Will cover Several techniques to make the best of this interesting situation :**
- **High pin counts? 1200 → 3000**
  - **What's the Problem?**
  - **What circuit design can contribute.**
  - **How Manufacture can contribute to the solution**
  - **Understanding the principles underlying the Channel routing technique. To Avoid sequential Lamination if possible.**

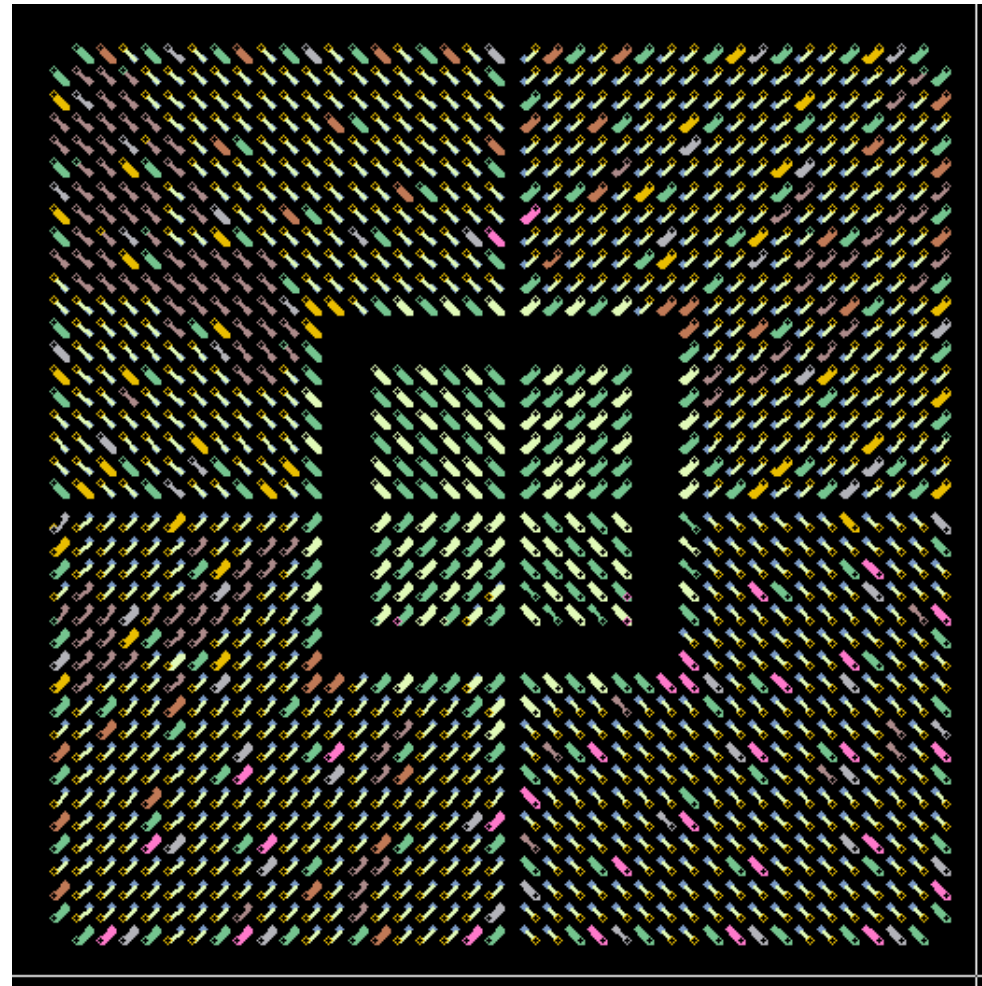
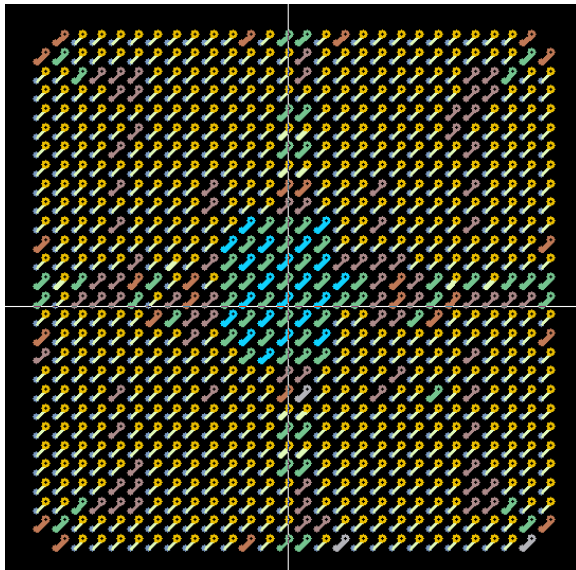
# High Pin Count BGA routing Techniques

- What's the Problem?

780 pins  $\rightarrow$  1700 pins

Avail. Exits  $\rightarrow$  linear

Required  $\rightarrow$  exponential



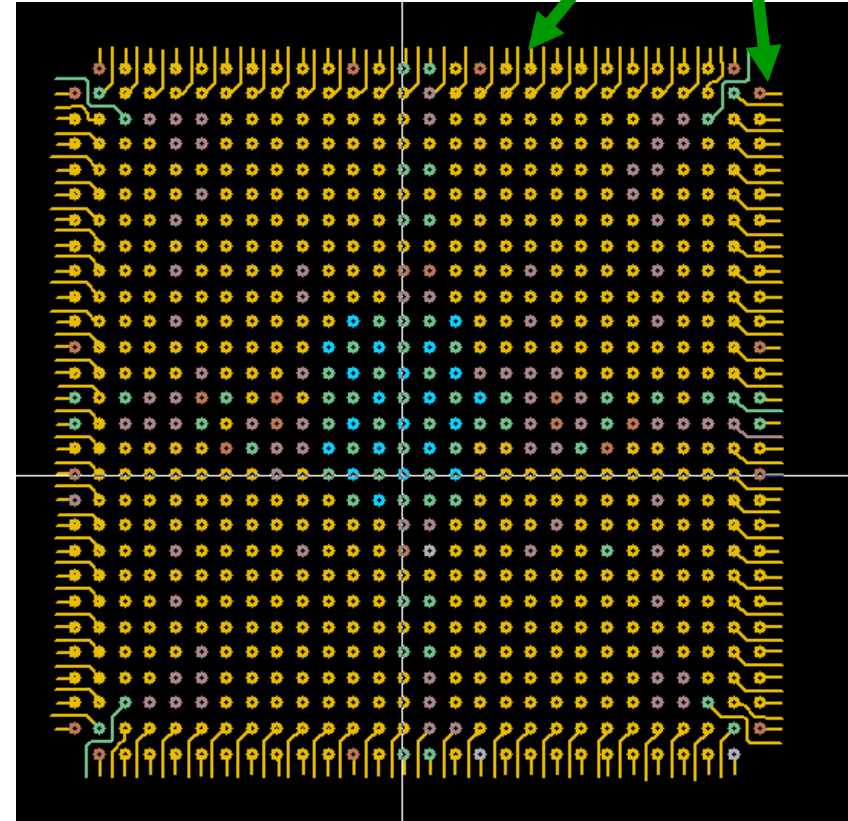
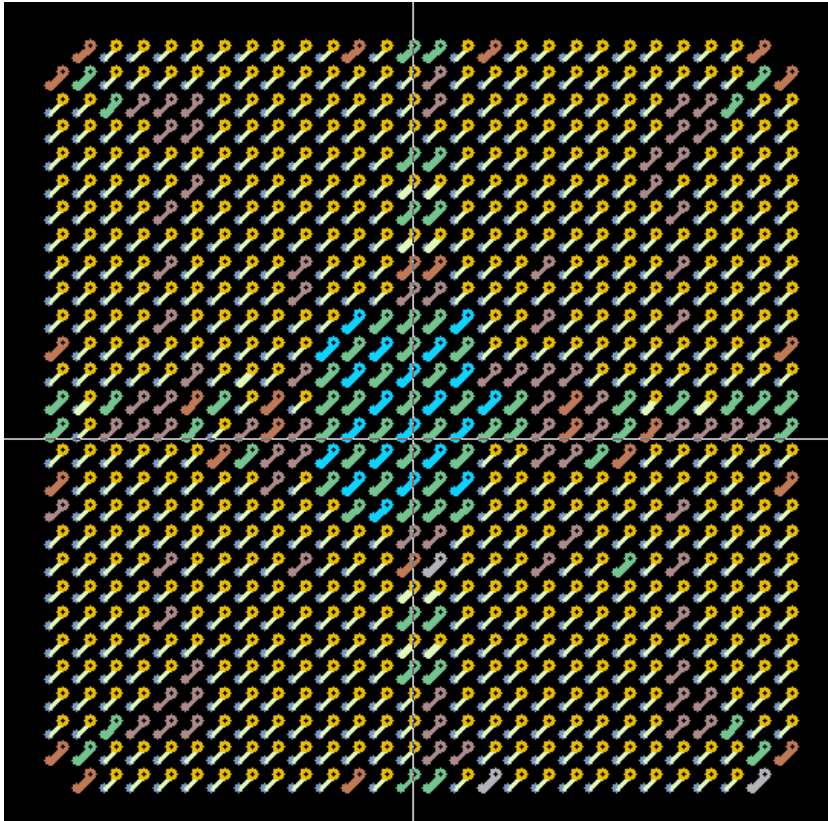
# High Pin Count BGA routing Techniques

What's the Problem?

Basic Dogbone 780 → 1st routing layer (1 between)

Basic straight out escape → gets the 2 outer perimeters

“FREE ONE”



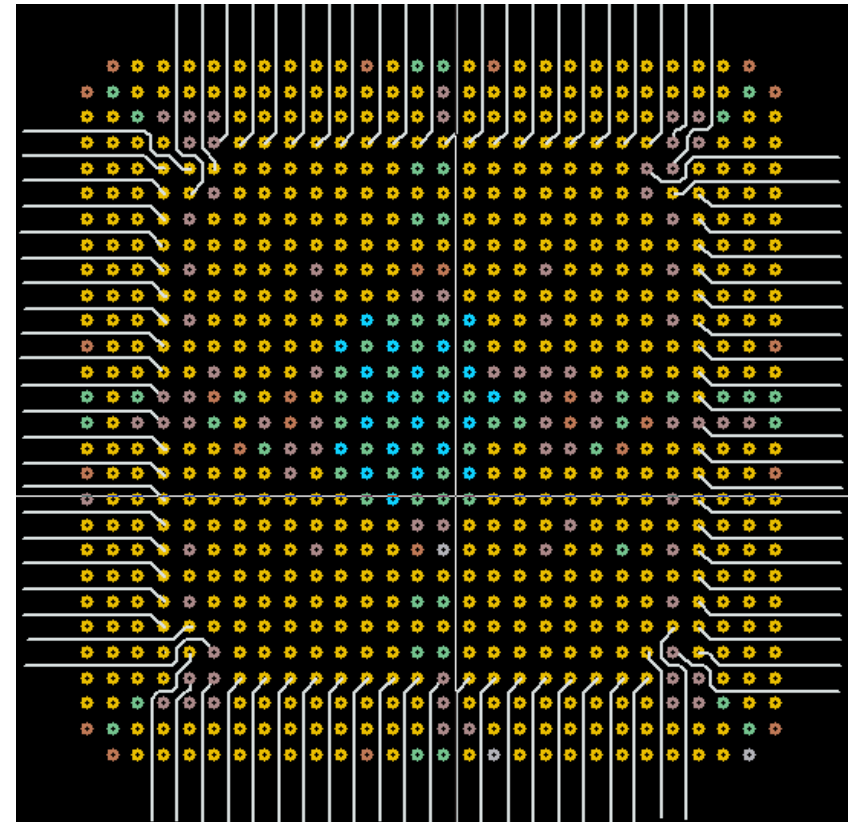
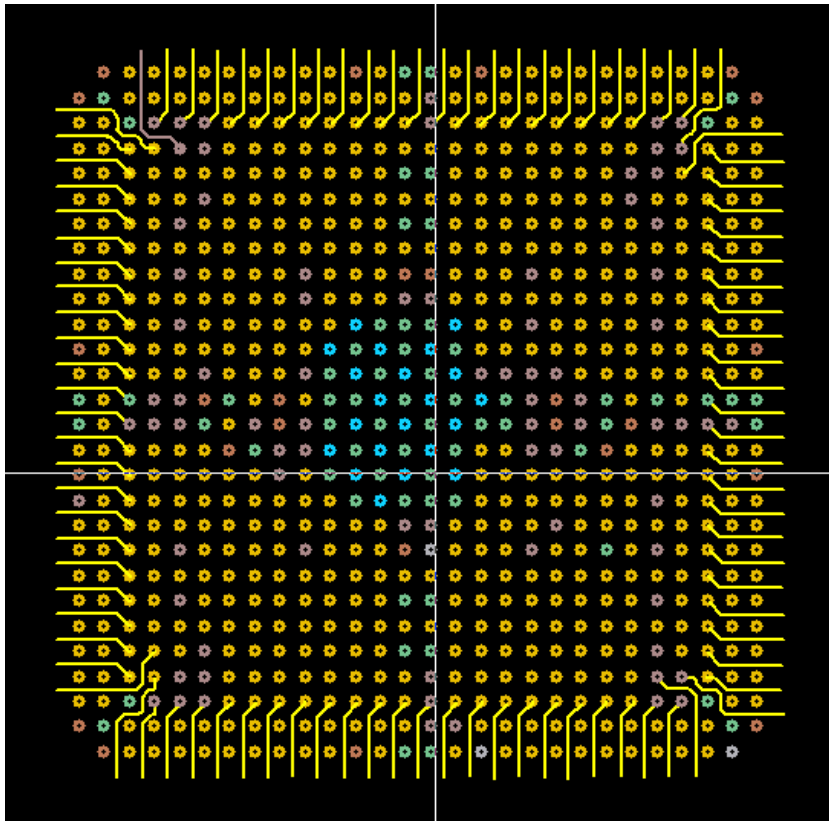
# High Pin Count BGA routing Techniques



**What's the Problem?**  
**2nd routing layer (1 between)**  
**gets the next outer perimeter**

**Basic Dogbone 780**

**3rd routing layer**  
**gets 1 more perimeter**



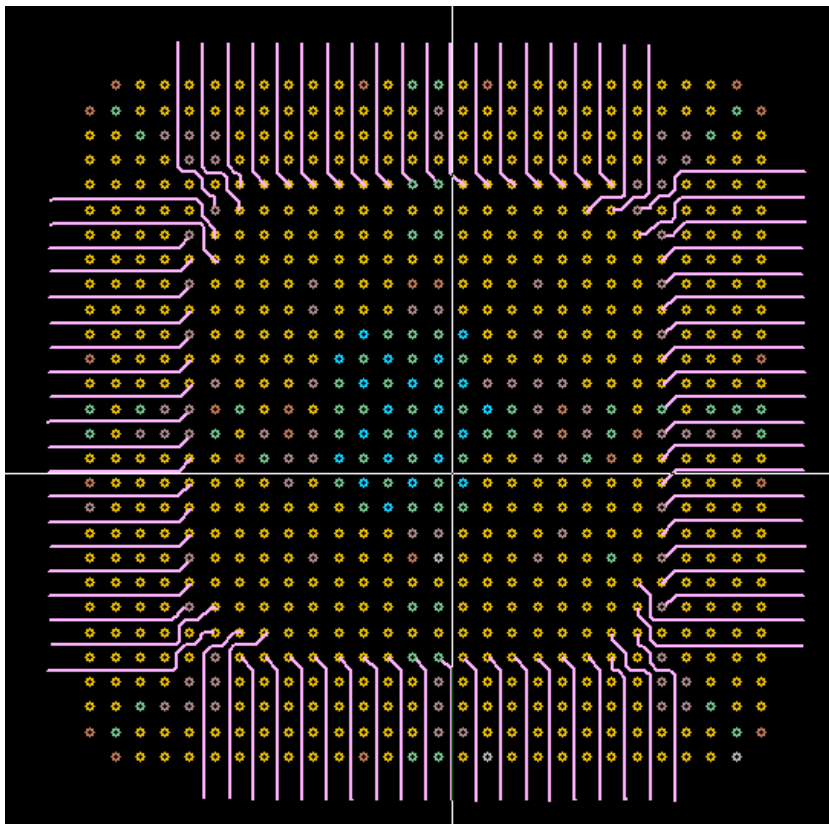
# High Pin Count BGA routing Techniques



**What's the Problem?**

**4th routing layer**

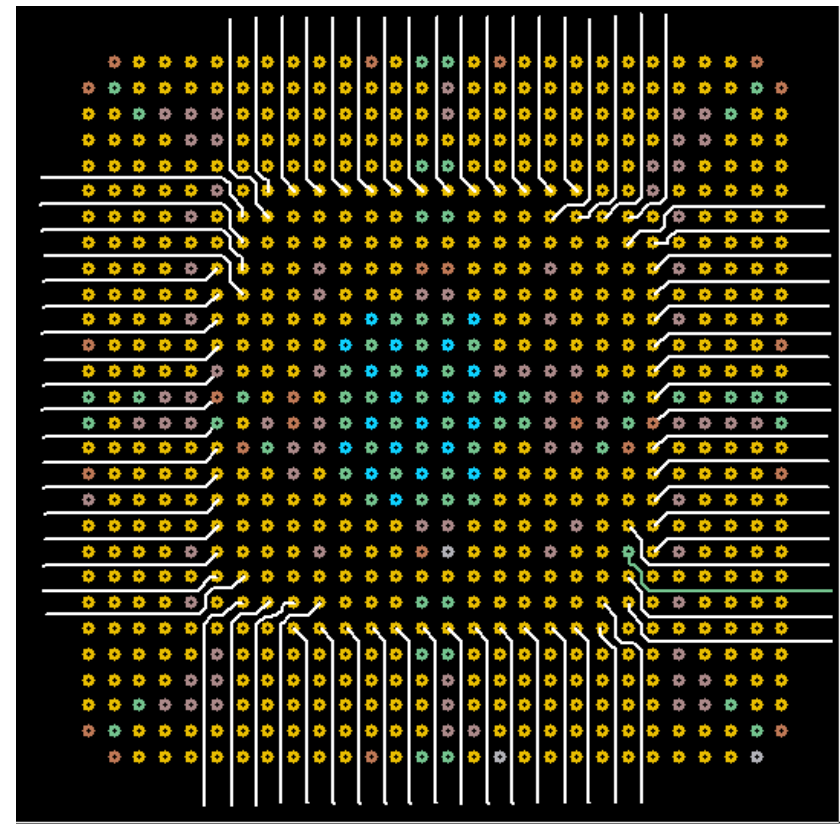
**gets 1 more perimeter**



**Basic Dogbone 780**

**5th routing layer**

**gets 1 more perimeter**



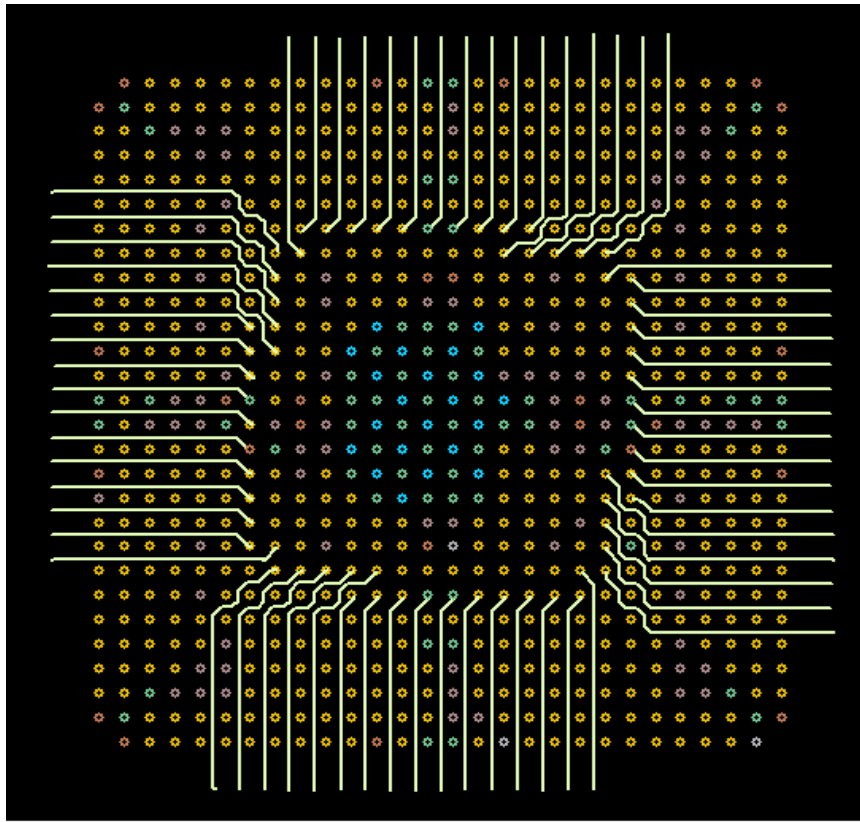
# High Pin Count BGA routing Techniques



**What's the Problem?**

**6th routing layer**

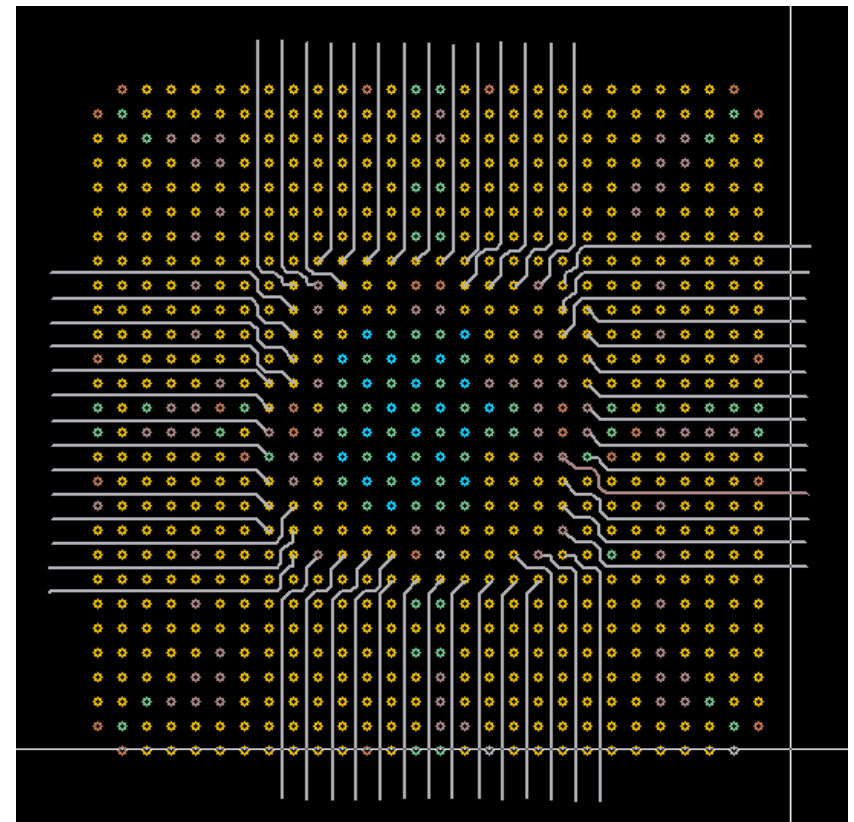
**gets 1 more perimeter**



**Basic Dogbone 780**

**7th routing layer**

**gets 1 more**



# High Pin Count BGA routing Techniques

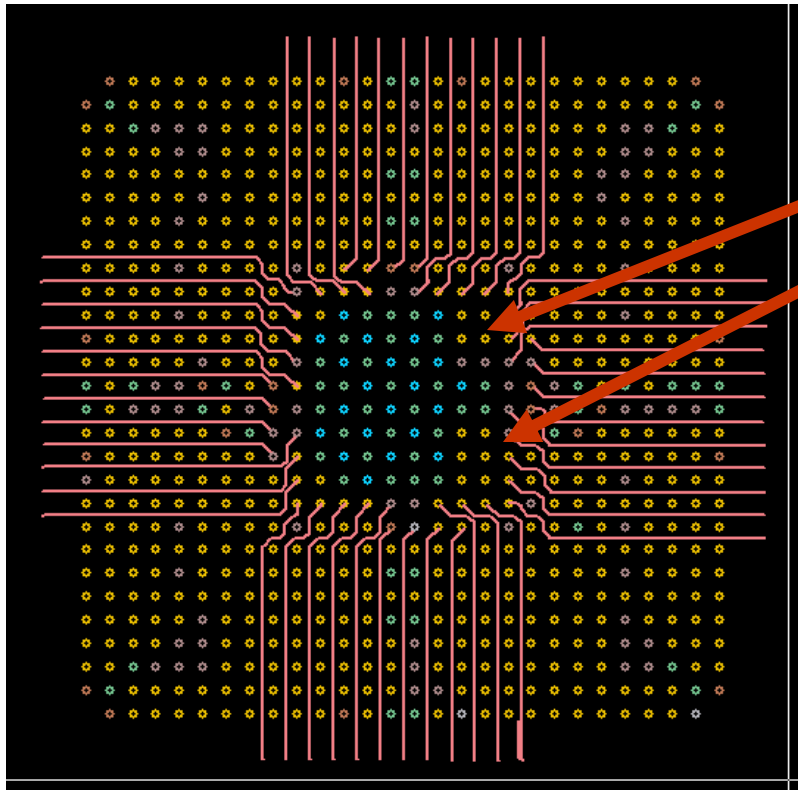
What's the Problem?

Basic Dogbone 780

8th routing layer

gets 1 more

With 8 layers not all pins exited !!



But we only have 8 layers and that should be enough?

Can the number of layers needed be calculated?



# High Pin Count BGA routing Techniques



- **Calculating the Min. # layers needed :**
  - On this 28 X 28 pin bga we saw that the outer most perimeter was “free”. We got 2 rings on the first layer used.
  - We had  $27 * 4$  (sides) between passage ways per layer to get to the pins that needed to exit. 108 between exits per layer.
  - If we apply the widely used flare-out/cross/plus-sign dogbone pattern 4 more exits on each of 4 sides (16 per layer) are added giving us 124 via between exits per layer.

# High Pin Count BGA routing Techniques

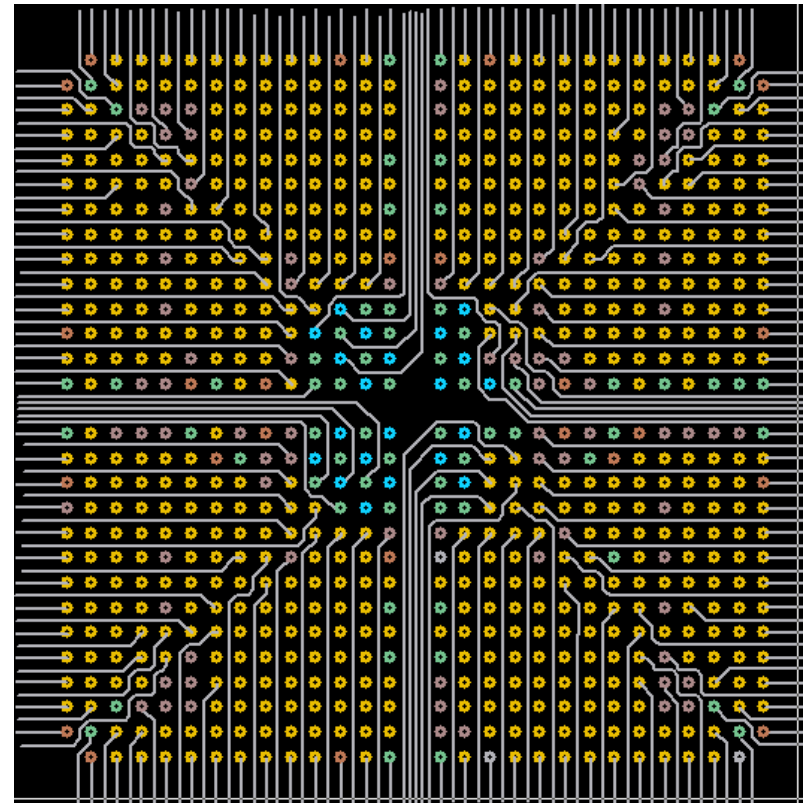
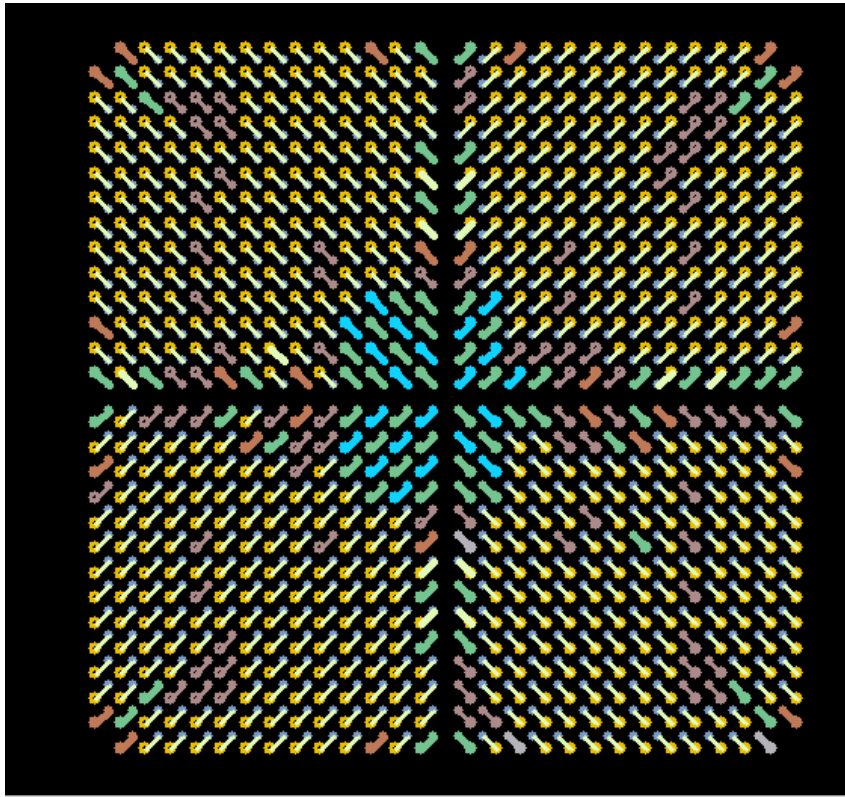


- **Calculating the Min. # layers needed :**
  - We have to get to  $26 * 26 = 676$  pins (max?)
- **Would 6 layers \* 124 = 744 be close?**
  - 5 layers \* 124 = 620 definitely not enough. (need 56 exits on layer 6)
  - Ignoring other factors (NC & PWR etc.) until later; see if the corner exits passages can be fully utilized; to see if this is on track.

# High Pin Count BGA routing Techniques

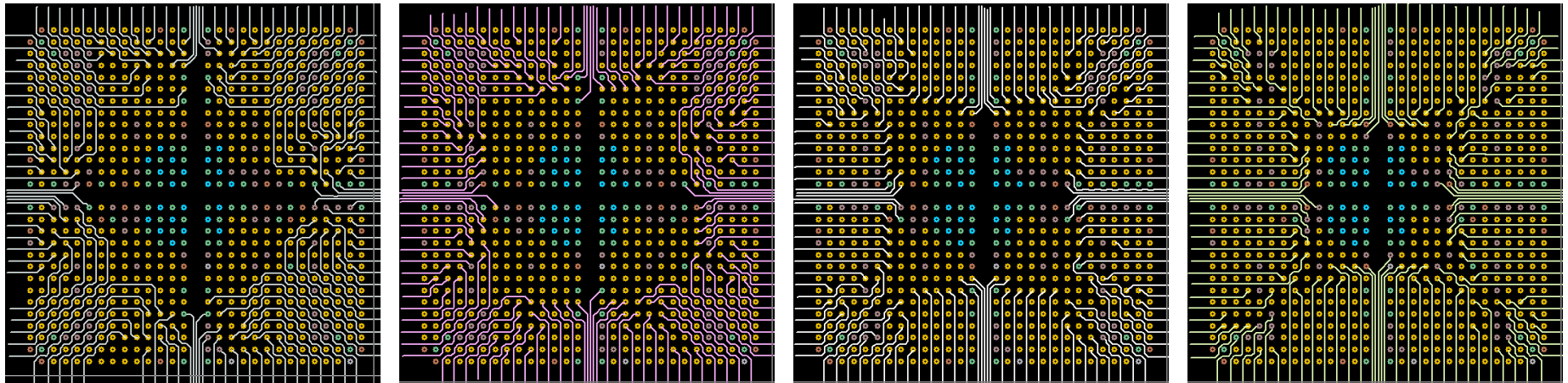


Flared Dogbone 780 → 1st routing layer (1 between)  
45 degree max. out exit → gets the 2 outer perimeters  
ALL 124 exits used.

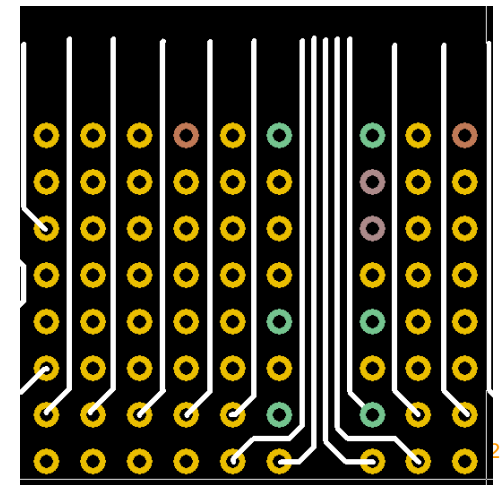
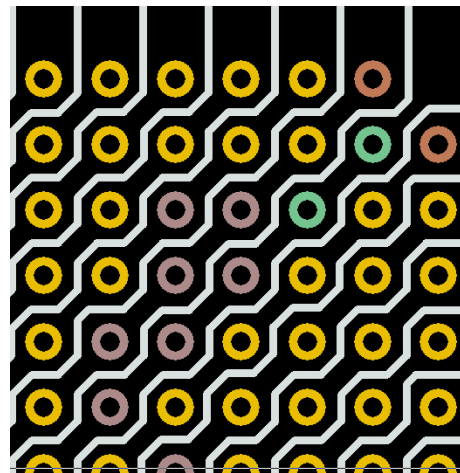


# High Pin Count BGA routing Techniques

All 124 possible exits used layer 2 through 5

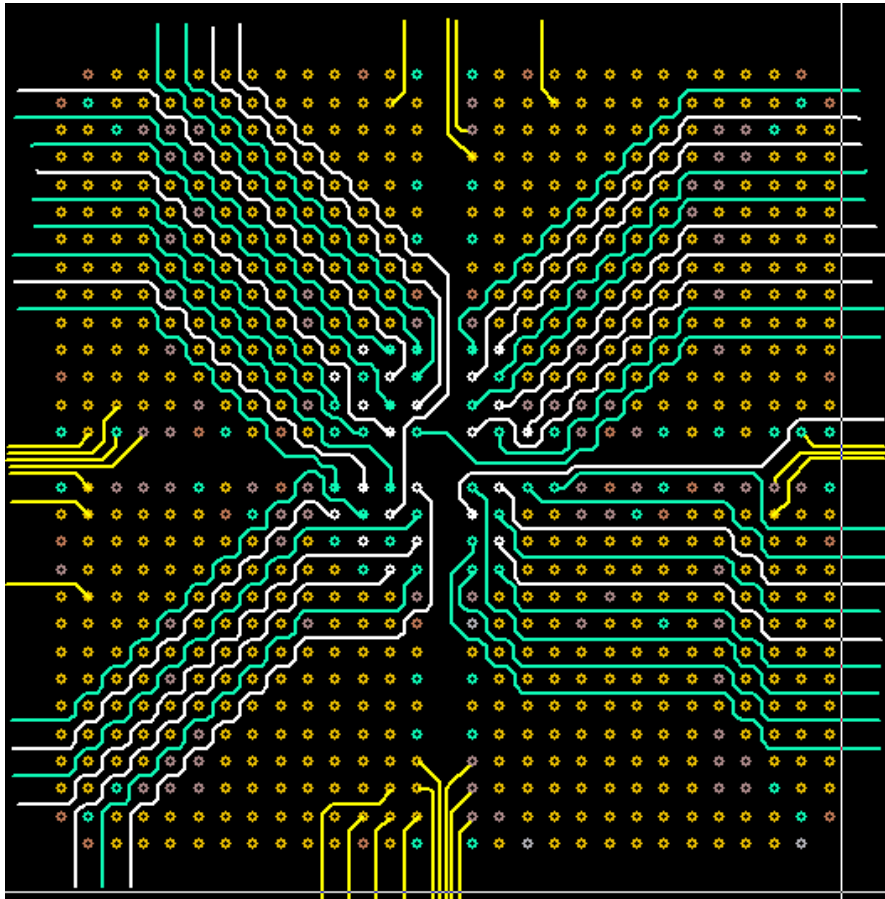


Notice the 45 degree routing required to utilize the corners.  
Also 5 between in “plus sign/cross”.



# High Pin Count BGA routing Techniques

layer 6 took the rest with the numbers in line with calculated required exits.



1. Notice we have power and nc vias being exited.
2. Not necessary if the power is supplied by negative plane layers.
3. We can adjust the calculation for these and see how much impact they have.

# High Pin Count BGA routing Techniques



- **Calculating the Min. # layers needed nc and pwr pins need not exit:**
  - flare-out/cross/plus-sign dog\_bone pattern gives us 124 via between exits per layer.
  - Need  $26 * 26 = 676$  pins total
  - subtract the nc and dummy net pins as well as the pwr and gnd pins that are fed by negative planes.
  - There are 76 nc/single\_net\_pin/dummy pins and 96 power and gnd pins (**excluding those in the outer perimeter ring of “free ones”**).
  - Need  $(26 * 26) - 172 = 504$  via between exits total. At 124 per layer we need?

# High Pin Count BGA routing Techniques

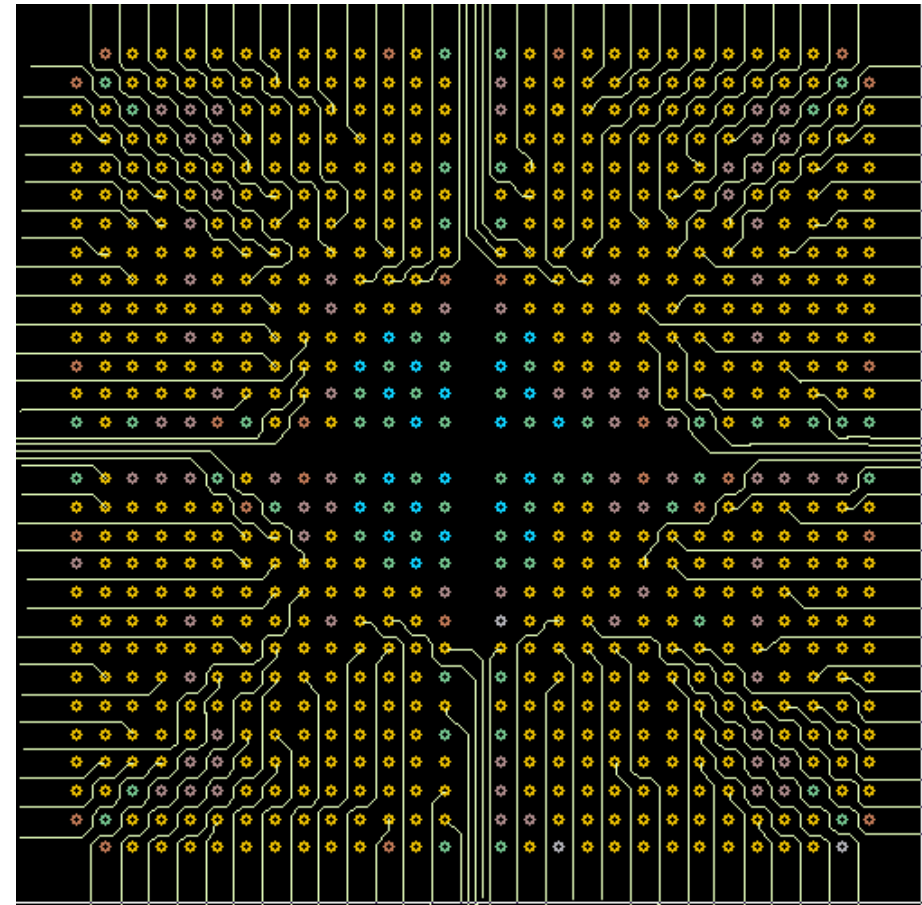
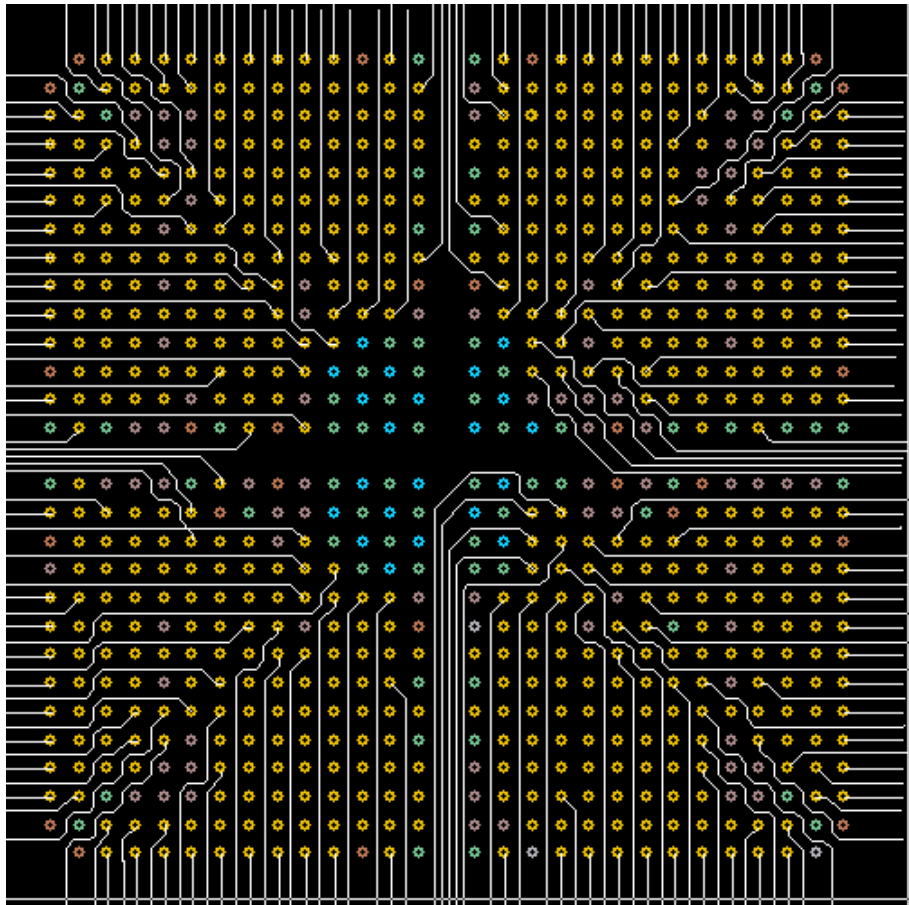


- **Calculating the Min. # layers needed nc and pwr pins need not exit: (Cont.)**
  - Need 504 via between exits total. At 124 per layer we need?
  - 4 layers gives 496 so 5 layers ARE NEEDED.
  - With 100% efficient exits we will only have 8 exits on the 5<sup>th</sup> layer.

# High Pin Count BGA routing Techniques



All 124 possible exits used layer 1 through 4

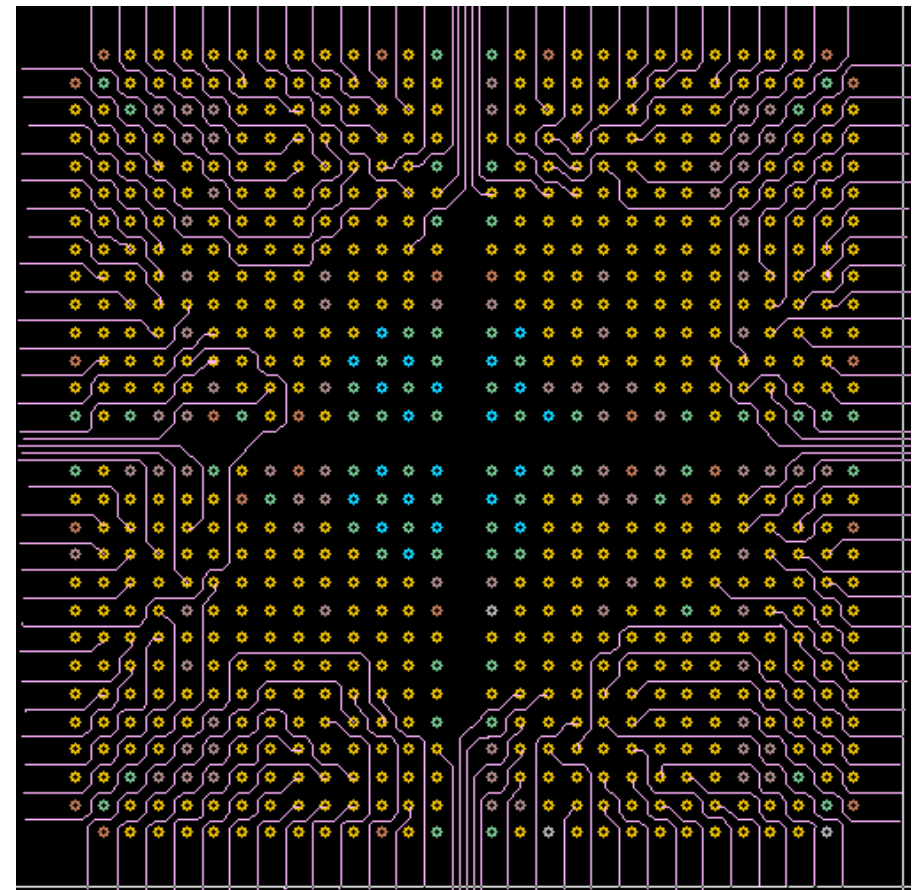
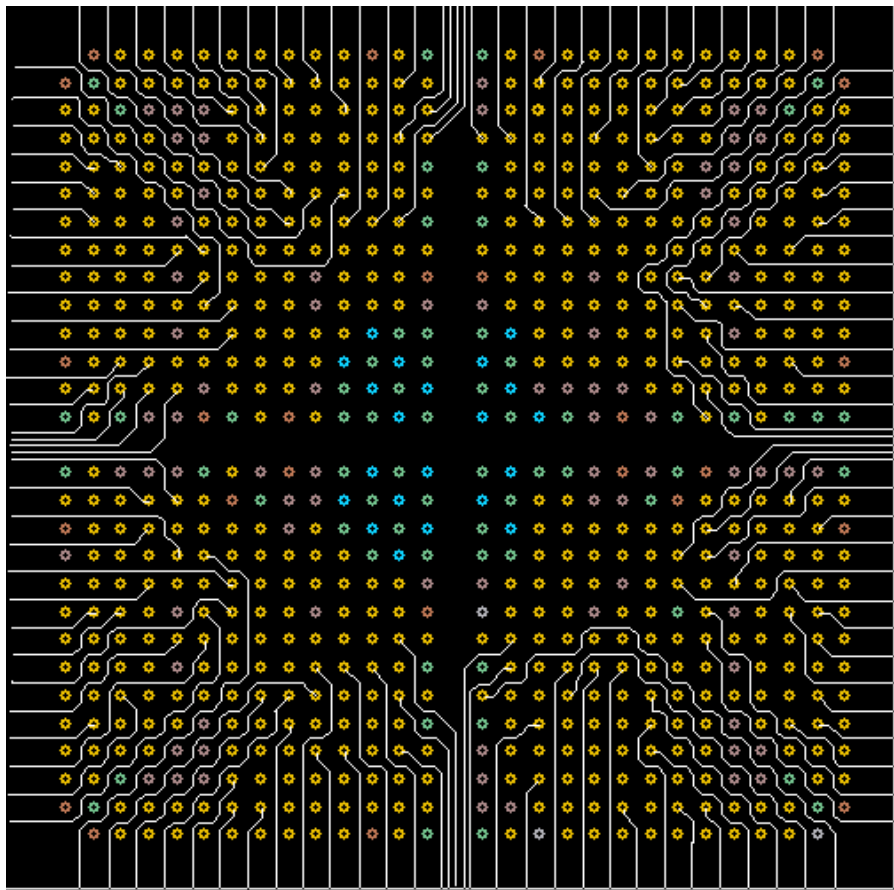




# High Pin Count BGA routing Techniques

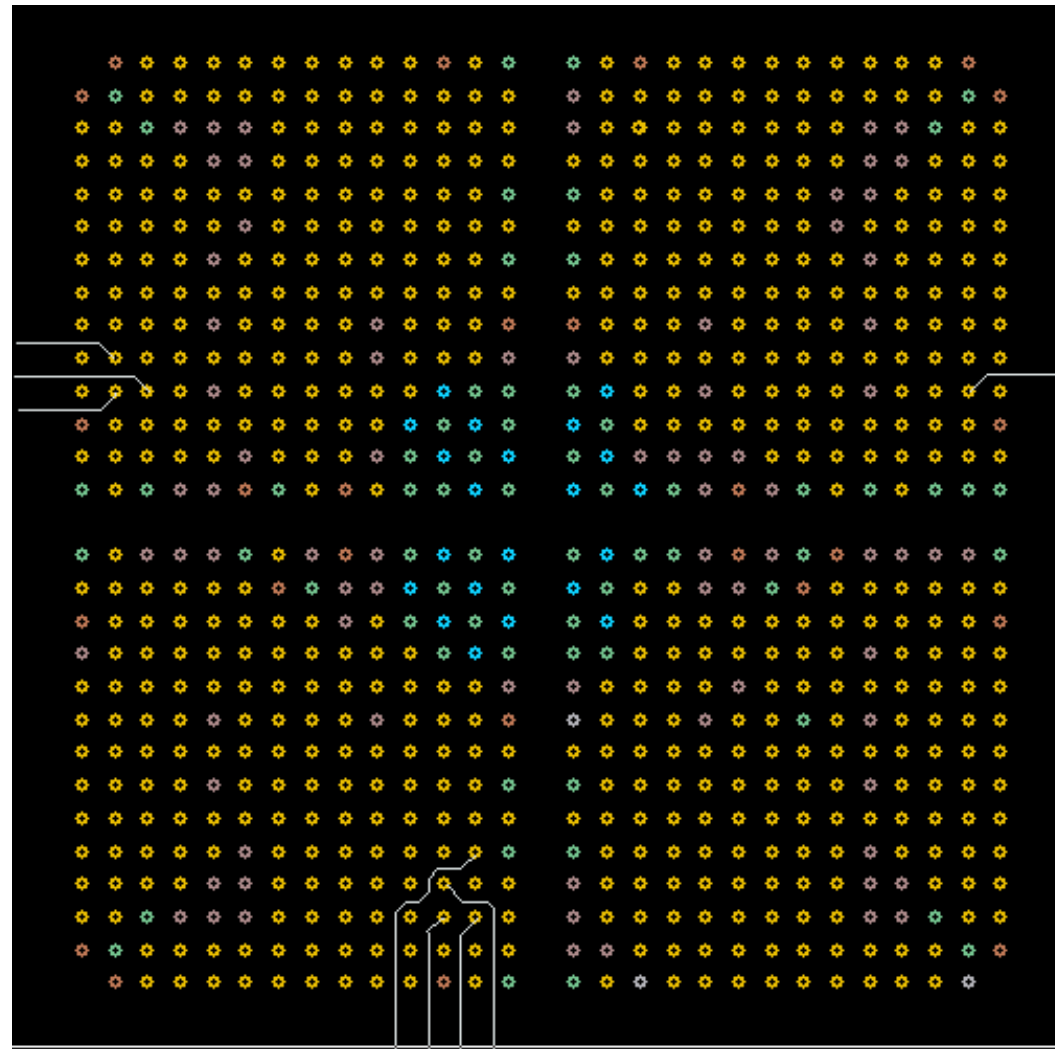


All 124 possible exits used layer 1 through 4



# High Pin Count BGA routing Techniques

Notice only 8 exits on the 5<sup>th</sup> layer.



# High Pin Count BGA routing Techniques Factors



- **Factors **increasing** number of exits required**
  - Multi\_rat pins as in daisy chained, ordered starburst nets, or just multi\_pin nets where the shortest Manhattan requires multiple rats to the pins.
  - Wider than nominal widths required for some nets in a 2 between technology situation.
  - Use\_layer rules that require more the max. possible exits per specified layers.
  - A requirement to exit nc or single\_net pins in order to get testpoint pitch greater than the bga pin pitch.
- **When these are quantified, the required number of layers calculation can be made allowing for them.**

# High Pin Count BGA routing Techniques Factors



- Factors **decreasing** the number of exits required
  - Connections between adjacent pins of the bga and/or with discretes on the bottom sharing a bga fanout via such as terminators.
  - Exits that can be solved on either the Top or Bottom layers.
  - Pin to pin Connections local to the bga on any layer.
  
- When these are quantified the required number of layers calculation can be made allowing for them.

# High Pin Count BGA routing Formula to calculate 100% layers utilization



- **Variables**

- **n** pin grid count ie. 28 in the case of the 780 example
- **FL** # of exits gained per layer by flared fanout for trace width used.
- **CH** # of exits gained per layer by Channel routing (explained later) fanout for trace width used. (Note exception 1<sup>st</sup> layer)
- **B** # of traces between bga fanout vias.
- **EXITS/LAYER =  $4B*(n-1) + FL + CH$**

# High Pin Count BGA routing Formula to calculate 100% layers utilization



## • Variables

- **PWR\_NC** = # of exits avoided by power fed from negative layers plus unconnected/single\_net\_pins. (excluding those in the “free ring”).
- **MULTI\_RAT** = total # of rats over 1 per pin that exit
- **INSIDE\_NET** total # of rats that connect within BGA (including TOP & BOTTOM) (excluding those in the “free ring”).
- **NEED\_EXITS** =  $(n*n) - 4*(n-1) - pwr\_nc + MULTI\_RAT - INSIDE\_NET$
- **NEED\_LAYERS** =  $NEED\_EXITS / EXITS/LAYER$  (+ 1 if remainder)

# 100% exit utilization table



| BGA GRID      | FLARE CHAN | TECH            | EXITS/LAY | PWR _NC | MULTI RAT + | INSIDE NET - | NEED EXITS | <u>NEED LAYERS</u> | EXITS OVER |
|---------------|------------|-----------------|-----------|---------|-------------|--------------|------------|--------------------|------------|
| 28X28<br>780  | NOT        | 1 BETW<br>5x5   | 108       | 0       | 0           | 0            | 676        | 7 (756)            | 80         |
| 28X28<br>780  | FL<br>+16  | 1 BETW<br>5x5   | 124       | 0       | 0           | 0            | 676        | 6 (744)            | 68         |
| 28X28<br>780  | FL<br>+16  | 1 BETW<br>5x5   | 124       | 172     | 0           | 0            | 504        | 5 (620)            | 116        |
| 28X28<br>780  | FL<br>+20  | 2 BETW<br>3 1/2 | 236       | 172     | 0           | 0            | 504        | 3 (708)            | 204        |
| 36x36<br>1296 | FL<br>+16  | 1 BETW<br>5x5   | 156       | 200     | 0           | 0            | 956        | 7 (1096)           | 140        |
| 42X42<br>1764 | FL<br>+16  | 1 BETW<br>5x5   | 180       | 250     | 0           | 0            | 1350       | 8 (1440)<br>9?     | 90<br>low  |
| 42X42<br>1764 | FL<br>+16  | 1 BETW<br>5x5   | 180       | 250     | +640        | -100         | 1890       | 11 (1980)<br>12?   | 90<br>low  |

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# High Pin Count BGA routing Circuit Design Techniques



- **What Circuit Design can contribute where POSSIBLE and BENEFICIAL (reduce required exits OR increase available exits):**
  - **Use series terminators with stub lengths that reach outside the bga array.**
  - **Use parallel terminators and decouplers that are small enough for under the bga placement.**
  - **Allow pwr/gnd via sharing where possible.**
  - **Gnd: and via share NC/dummy/single net pins where possible.**
  - **Allow no fanout on NC pins particularly on the (outer – 1) perimeters of the array.**



# High Pin Count BGA routing Circuit Design Techniques



- **What Circuit Design can contribute where POSSIBLE and BENEFICIAL ( To reduce required exits OR increase available exits): (Cont. 1)**
  - **Make gate assignments to fully utilize that “free outer perimeter ring”.**
  - **On nets with controlled impedance requirements, define acceptable top/bottom lengths if possible for external terminator hook-up**
  - **Allow the use of virtual vias outside to get to daisy (2 rat pins) with 1 exit, with appropriate stub and gate assignment.**

# High Pin Count BGA routing Circuit Design Techniques



- **What Circuit Design can contribute where POSSIBLE and BENEFICIAL ( To reduce required exits OR increase available exits): (Cont. 2)**
  - **Can? (neck down and reduced clearance to get 2 between) be tolerated to in through the first 3 or 4 perimeters. (5X5 -> 3 ½X 3 ½).**
  - **Identify pins that are NOT connected inside to bga therefore do not need a dog\_bone or testpoint.**

# High Pin Count BGA routing Manufacturing Techniques



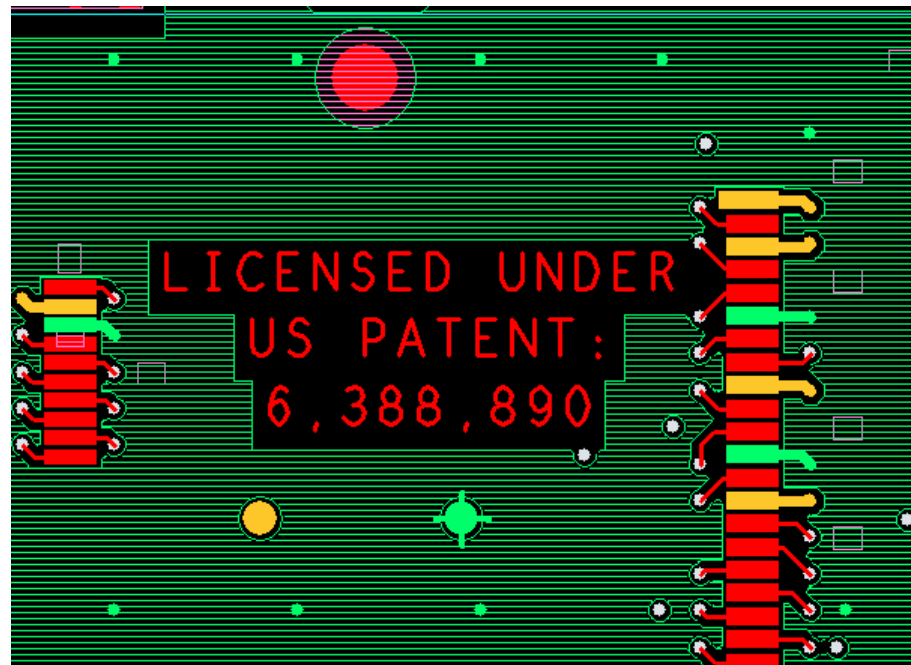
- **What Manufacturing can contribute where POSSIBLE and BENEFICIAL ( To reduce required exits OR increase available exits):**
  - **Achieve high yield on (neck down and reduced clearance to get 2 between) be tolerated to in through the first 3 or 4 (few) perimeters. (5X5 -> 3 1/2X 3 1/2).**
  - **Apply testing techniques such as X-RAY inspection that avoid the need for testpoints on NC pins.**
  - **Tolerate identified 0.1 mil clearance reductions where these allow an extra exit. Example 4.8 via to trace in in 5x5 tech where we find a gap of 54.8 mils and need 55 to get 5 between. (basically a verification issue)**

# High Pin Count BGA “CHANNEL ROUTING” Technique



**CHANNEL ROUTING** as covered by:

**Nortel Networks' intellectual property rights', including but not limited to US Patents 6,388,890 and 6,545,876.**



# High Pin Count BGA “CHANNEL ROUTING” Technique



- As we have seen, the Flared fanout pattern gives us 16 additional exits per routing layer providing **128 additional exits** on an 8 routing layer design.
- And someone thought it would really be great, if we could get more of these wide Channels on large BGA's.
- Channel routing is a technique to do just that.

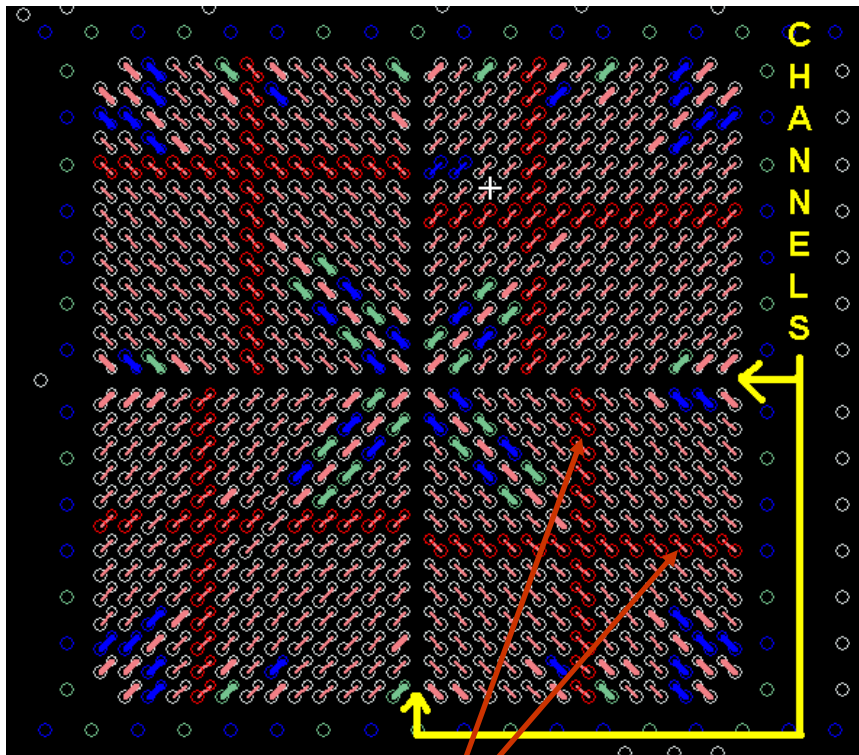
# High Pin Count BGA “CHANNEL ROUTING” Technique



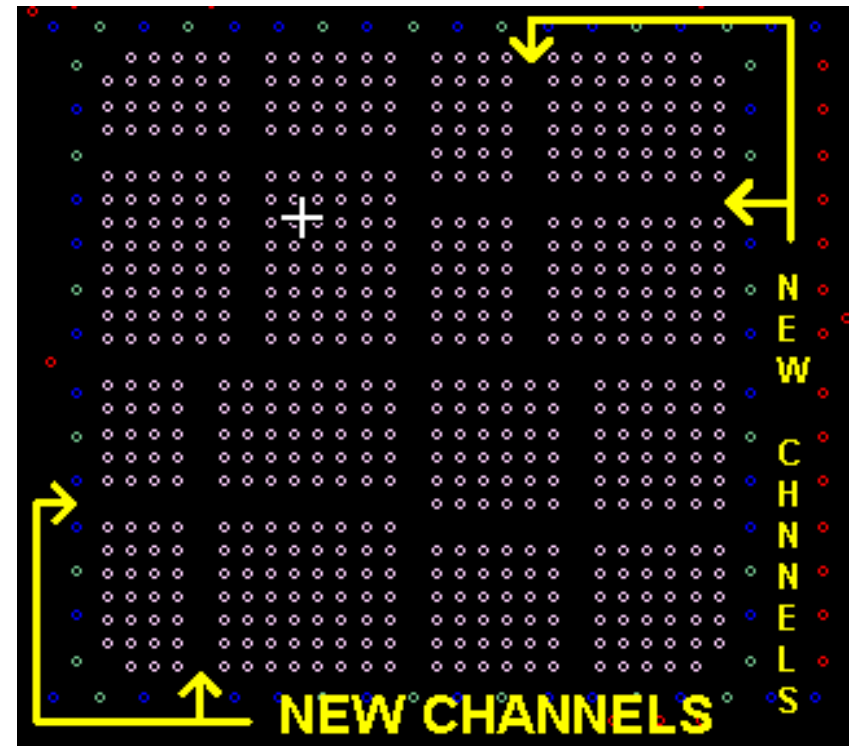
- **The WHAT and HOW of channels, once understood, is really a very simple concept in principle. A very few shallow blind vias provide a big difference in routing access to large BGA's. (reduces layer count costs)**
- **This can be achieved without incurring the cost increase of sequential lamination.**
- **Only uses a very few controlled depth drilled blind vias and all the rest standard through hole vias.**

# High Pin Count BGA “CHANNEL ROUTING” Technique

Without channel routing



With channel routing



Must become blind vias or be omitted to create the additional channels

# High Pin Count BGA “CHANNEL ROUTING” Technique



- **Finding channel location possibilities:**
- **Search for rows and columns in each quadrant that combined, will create a channel in the required pattern either cross or L's by using the following in combination:**
  1. **Not providing unused pin fanouts.**
  2. **Sharing pwr/gnd to adjacent pin via fanouts**
  3. **Using pwr/gnd blind vias to that first pwr/gnd layer in**
  4. **Using blind vias for nets that are not constrained to be not allowed on that 2<sup>nd</sup> layer in or are pair members.**
  5. **Start with optimal choice (centered).**



# High Pin Count BGA “CHANNEL ROUTING” Technique



- Blind signal & pwr/gnd vias that create the channels

Best

Workable

Nice to avoid

## Suggested Stack-ups



OR



# High Pin Count BGA “CHANNEL ROUTING” Technique



- **Calculating the Min. # layers needed (on the 780 pin bga) with everything as previously, “plus channel routing”.**
  - **Each additional channel provides 3 more exits on all routing layers except the first one where the blind vias terminate (total of 24 per subsequent routing layer with the cross pattern).**
  - **124 via between exits on the blind via layer.**
  - **148 via between exits on rest of the routing layers.**
  - **As before we still need 504 via between exits total.**

# High Pin Count BGA “CHANNEL ROUTING” Technique



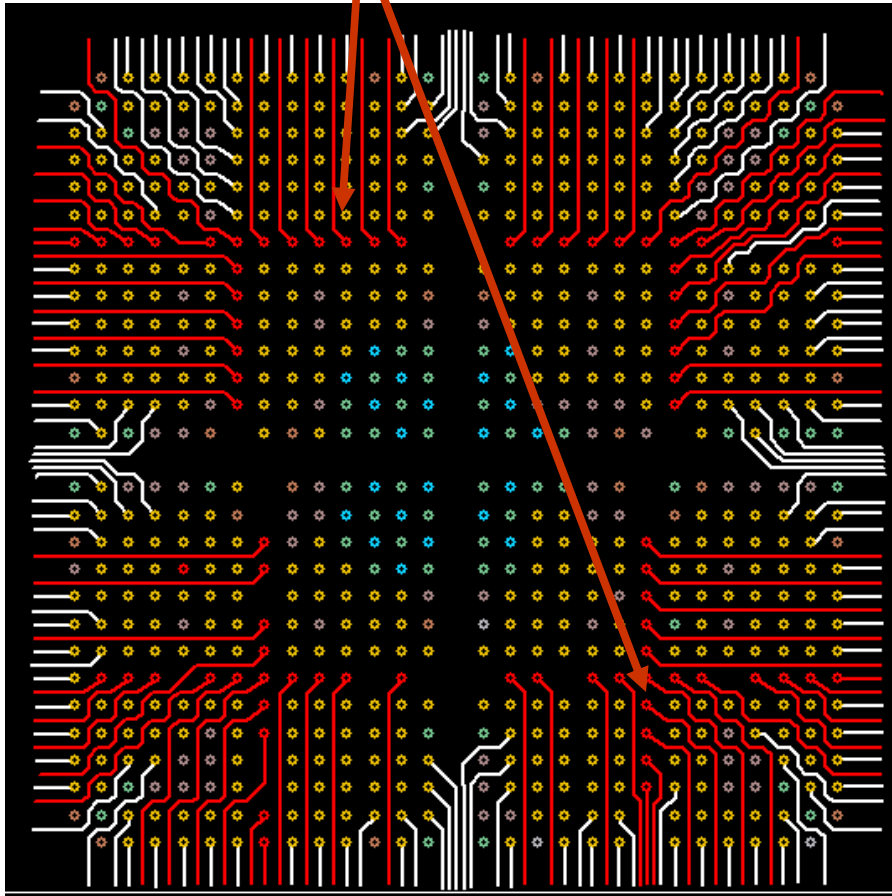
- **Calculating the Min. # layers needed (on the 780 pin bga) with everything as previously, “plus channel routing”.**
  - **Need 504 via between exits total. At 124 on the blind layer we need 380 on the lower routing layers.**
  - **3 more gives us  $3 \times 148$  or 444 so 4 routing layers should do it with 64 to spare.**
  - **(100% efficient exits utilization)**

# High Pin Count BGA

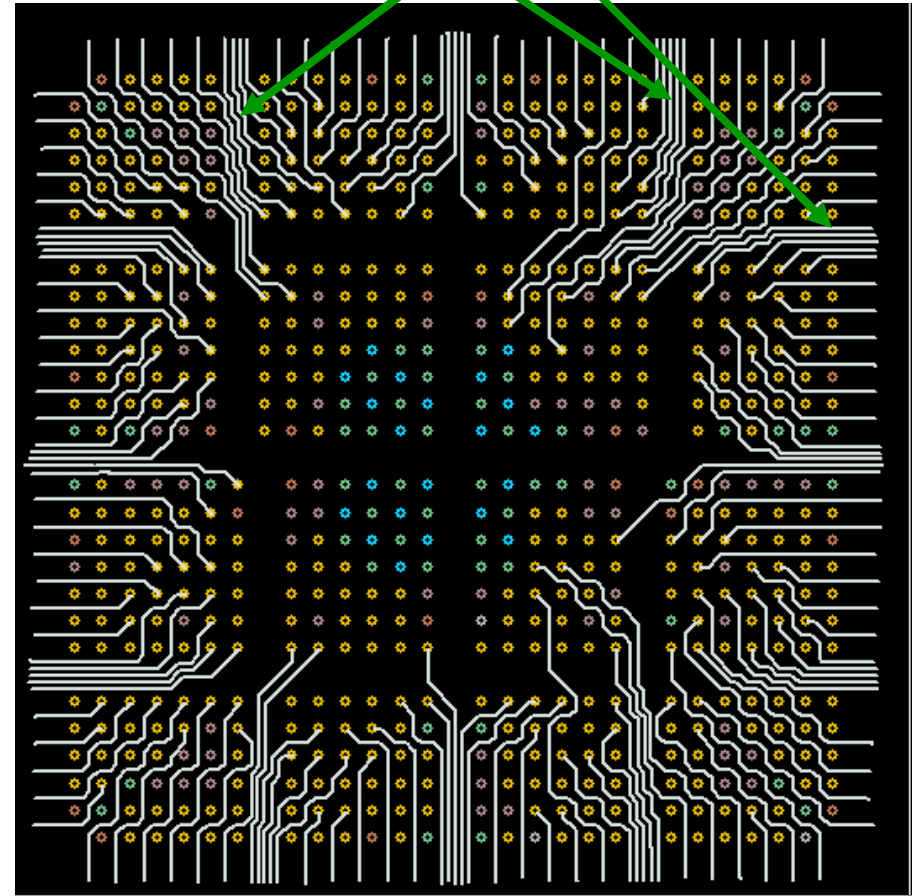
## “CHANNEL ROUTING” Technique



All 124 possible exits used  
(1<sup>st</sup> layer) **Note blind via exits**



All 148 possible exits used  
(2<sup>nd</sup> layer) **Channels utilized**

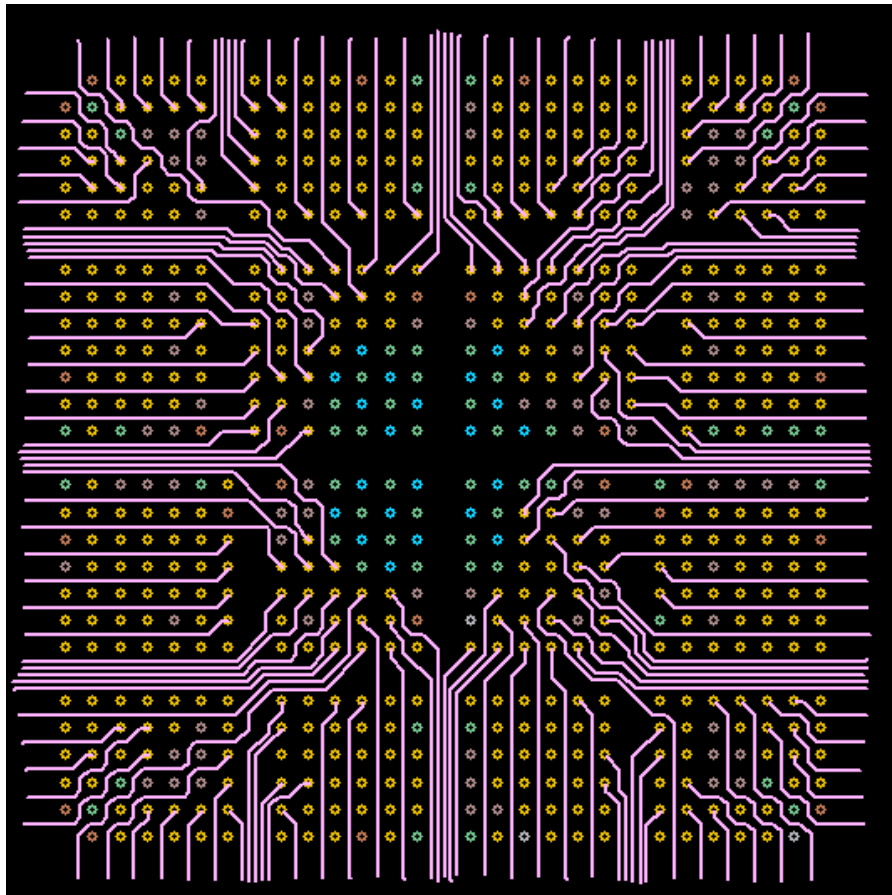


# High Pin Count BGA “CHANNEL ROUTING” Technique

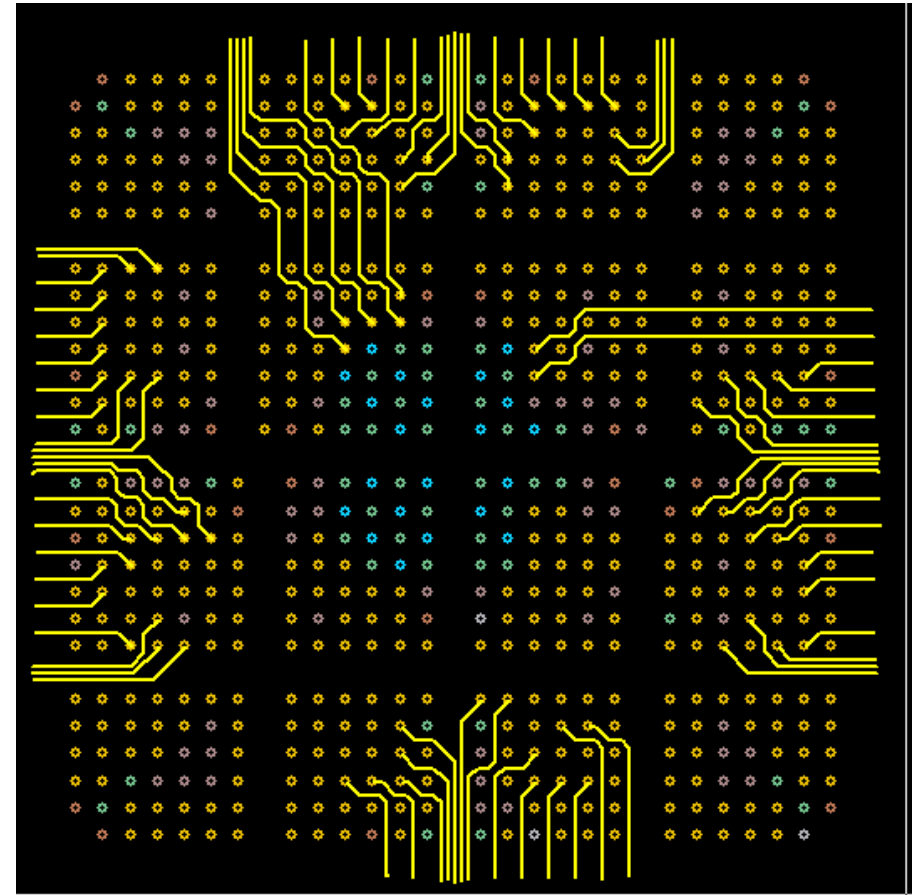


All 148 possible exits used

(3rd layer) Channels utilized



(4th layer) only needed some



# 100% exit utilization table



| BGA GRID      | FLARE CHAN    | TECH          | EXITS/LAY    | PWR /NC | MULTI RAT + | INSIDE NET - | NEED EXITS | <u>NEED LAYERS</u> | EXITS OVER |
|---------------|---------------|---------------|--------------|---------|-------------|--------------|------------|--------------------|------------|
| 28X28<br>780  | FL<br>+16     | 1 BETW<br>5x5 | 124          | 172     | 0           | 0            | 504        | 5 (620)            | 116        |
| 28X28<br>780  | FL+ CH<br>+40 | 1 BETW<br>5x5 | 124 &<br>148 | 172     | 0           | 0            | 504        | 4 (568)            | 64         |
| 36x36<br>1296 | FL<br>+16     | 1 BETW<br>5x5 | 156          | 200     | 0           | 0            | 956        | 7 (1096)           | 140        |
| 36x36<br>1296 | FL +CH<br>+40 | 1 BETW<br>5x5 | 156<br>180   | 200     | 0           | 0            | 956        | 6 (1056)           | 100        |

# 100% exit utilization table



| BGA GRID      | FLARE CHAN     | TECH          | EXITS/LAY  | PWR /NC | MULTI RAT + | INSIDE NET - | NEED EXITS | <u>NEED LAYERS</u> | EXITS OVER |
|---------------|----------------|---------------|------------|---------|-------------|--------------|------------|--------------------|------------|
| 42X42<br>1764 | FL<br>+16      | 1 BETW<br>5x5 | 180        | 250     | 0           | 0            | 1350       | 8 (1440)<br>9?     | 90<br>low  |
| 42X42<br>1764 | FL +CH<br>+40  | 1 BETW<br>5x5 | 180<br>204 | 250     | 0           | 0            | 1350       | 7 (1404)<br>8?     | 54<br>low  |
| 42X42<br>1764 | FL<br>+16      | 1 BETW<br>5x5 | 180        | 250     | +640        | -100         | 1890       | 11 (1980)<br>12?   | 90<br>low  |
| 42X42<br>1764 | FL +CH<br>+ 40 | 1 BETW<br>5x5 | 180<br>204 | 250     | +640        | -100         | 1890       | 10 (2016)          | 126        |

# 100% exit utilization table



| BGA GRID      | FLARE CHAN   | TECH            | EXITS/LAY  | PWR /NC | MULTI RAT + | INSIDE NET - | NEED EXITS | <u>NEED LAYERS</u> | EXITS OVER |
|---------------|--------------|-----------------|------------|---------|-------------|--------------|------------|--------------------|------------|
| 52X52<br>2704 | FL<br>+16    | 1 BETW<br>5x5   | 220        | 300     | +1000       | -200         | 3497       | 16 (3520)<br>17?   | 23<br>low  |
| 52X52<br>2704 | FL<br>+20    | 2 BETW<br>3 1/2 | 428        | 300     | +1000       | -200         | 3497       | 9 (3852)           | 355        |
| 52X52<br>2704 | FL+CH<br>+44 | 2 BETW<br>3 1/2 | 428<br>452 | 300     | +1000       | -200         | 3497       | 8 (3592)           | 95         |



# High Pin Count BGA

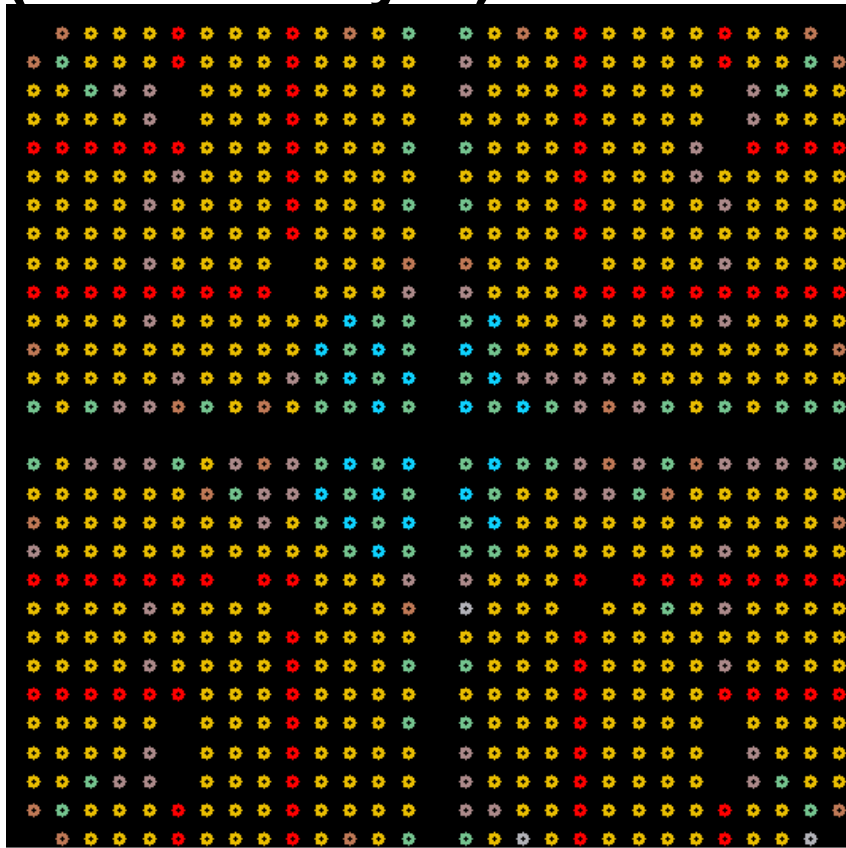
## “CHANNEL ROUTING” Technique



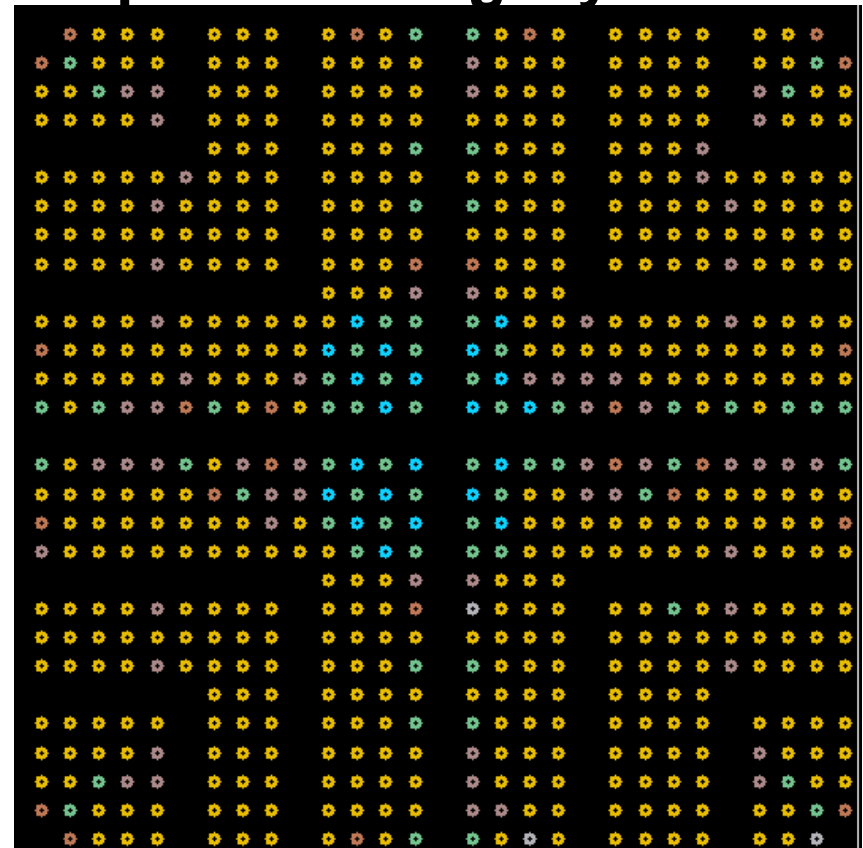
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We have looked at the cross pattern, other patterns are possible such as 2 L's per quadrant, and others

(bind via layer)



subsequent routing layers



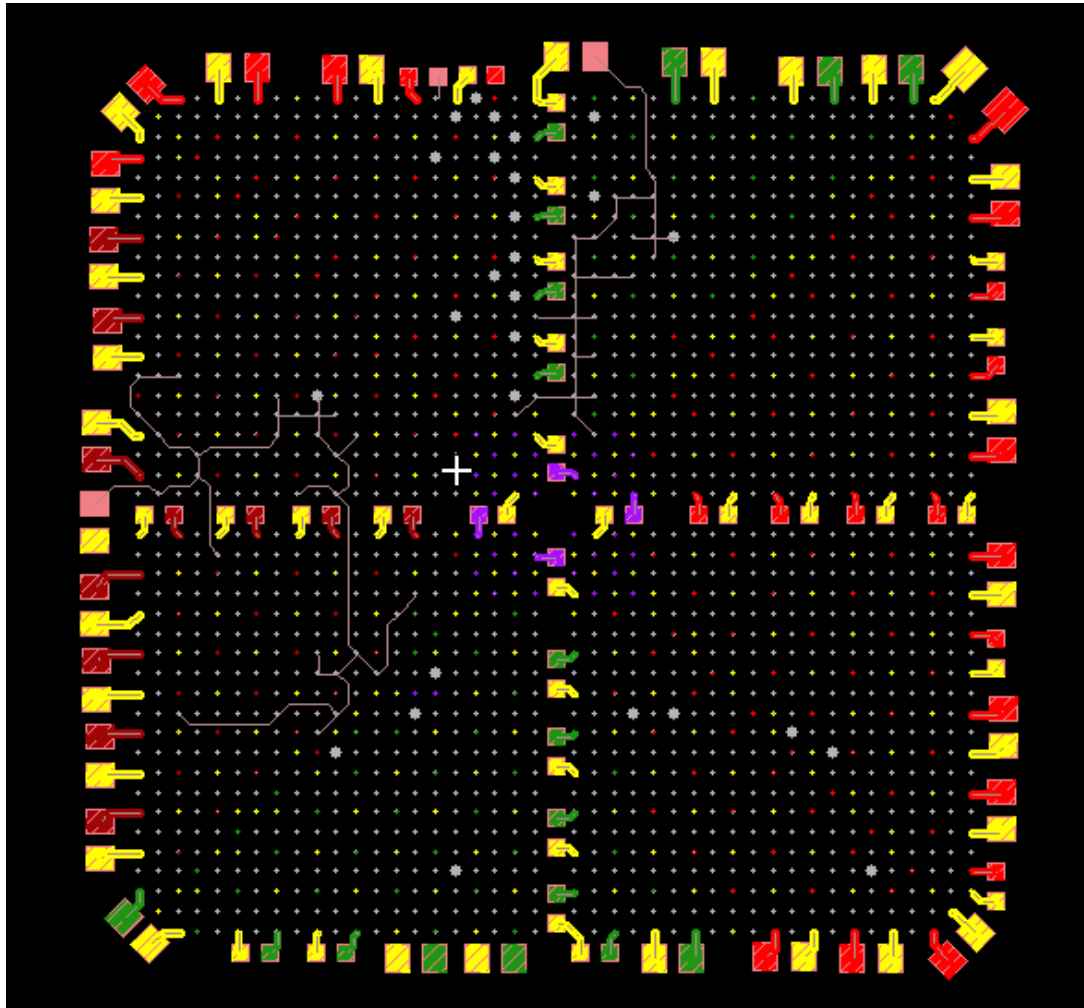
# High Pin Count BGA “CHANNEL ROUTING” Technique



- Clearly the additional channels gave us 1 routing layer reduction and usually on high\_speed designs, a gnd layer goes with it giving a 2 layer reduction.
- There is another effect that is less obvious at first :
  - The additional channel spaces on the bottom permits the placement of MORE discrettes under, which reduces the parking lot, and increases the local routes that need no exit.

# High Pin Count BGA “CHANNEL ROUTING” Technique

Under Traditional flared pattern 1700 pin BGA

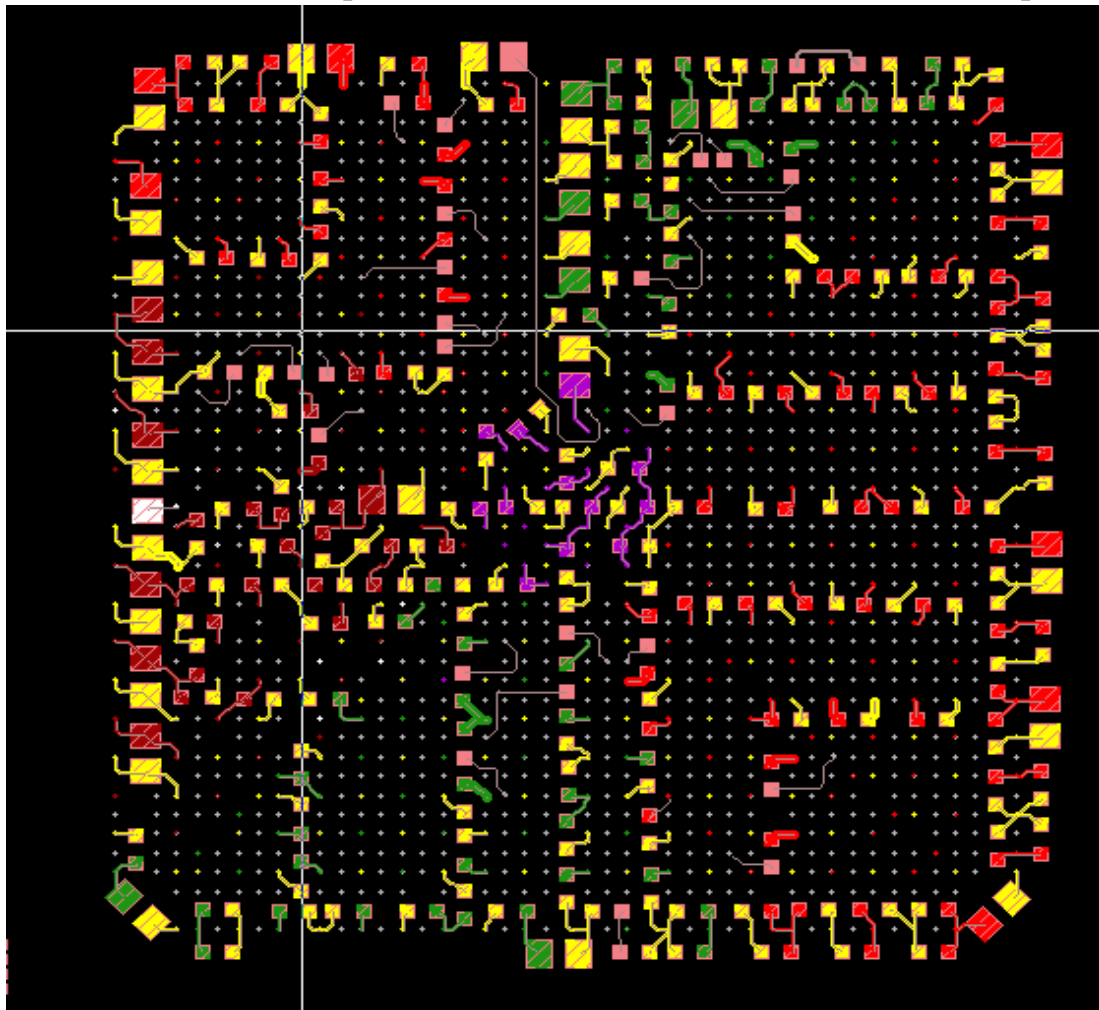


**58 DISCRETES**  
connected under  
the BGA sharing  
**116 VIAS.**

# High Pin Count BGA “CHANNEL ROUTING” Technique



L channel pattern with extended perimeter 1700 pin BGA



**183 DISCRETES**  
connected under  
the BGA sharing  
**366 VIAS**  
compared to 116.

**More than 3 times**  
as much sharing

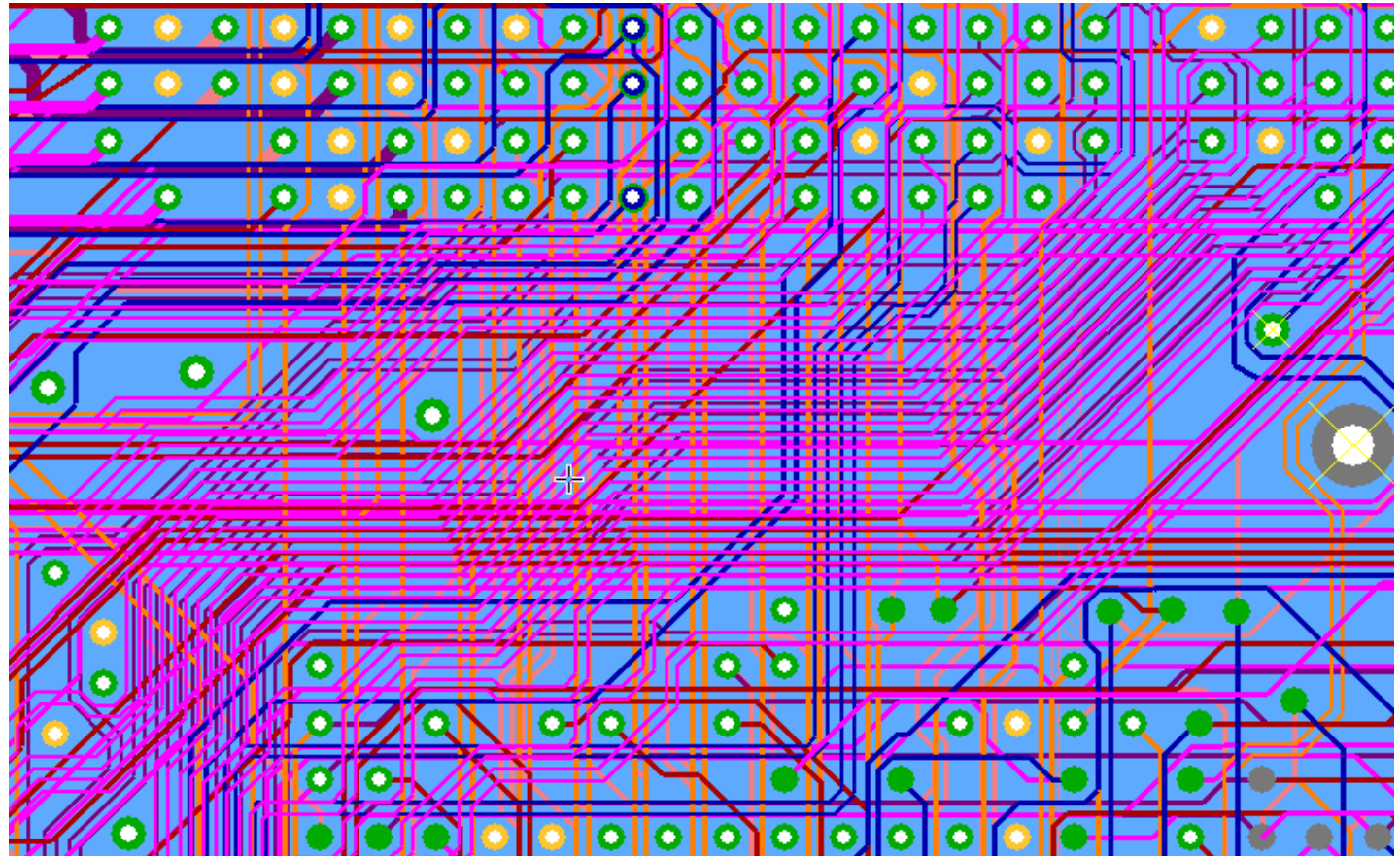
# High Pin Count BGA “CHANNEL ROUTING” Technique



Improved access between large bga's by putting the discrettes in the Bottom channels

Moving cars from the parking lots between big buildings into basement parking

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# High Pin Count BGA “CHANNEL ROUTING” BENEFITS



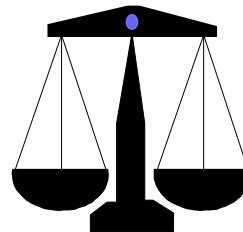
- **Reduced board cost:**
  - 14 layer -> 12 layer (allowing blind via channel cost increase) \$57.00 -> 50.56 savings **\$6.44**
  - 14 layer -> 10 layer (allowing blind via channel cost increase) \$57.00 -> 38.55 savings **\$18.45**
  - When we look at reducing a (1700 pin bga) 28 layer to 22 and/or avoiding sequential lamination or avoiding NOT FEASIBLE, THE SAVINGS MAY BE THE PROJECT.

# High Pin Count BGA “CHANNEL ROUTING” BENEFITS



- **Signal integrity improvement:**
  - Moving the discretes decouplers and terminators closer to their jobs makes them more effective.
  - Reducing the routing layer count can allow needed sandwiching with gnd layers on high speed designs.
  - The additional channels allow more diff pairs to maintain their optimal gap in cases where they do not form a nice 2 between pattern in the bga.

– **Cost saving**



**signal integrity**

# High Pin Count BGA “CHANNEL ROUTING” REALITY?



- **We have experienced:**
  - High 20's layers reduced by 6 layers
  - Low 20's layers reduced by 4 layers
  - Teens reduced by 2 layers.
- **Results should get even better with increased awareness of what factors influence layer count on large bga's, by everyone.**
- **We are now in the 80 to 90% range in terms of the full utilization of all exits on BGA's whether or not channel routing techniques are used.**
- **Discretes under save 1 or 2 layers**



# Bye

## If no more questions then

