(13) Update on Ghost Busters Preparing the board for Specctra

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International Cadence Usergroup

Ghost Content

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- A look at some current Specctra **"things that go thump in the night" And some Known exorcisms**
- The connector that auto connects fine in 14.1 not in 14.2 for **no earthly reason**
- **Strange bends & unexpected flow disruption**
- Taking a **life time** to load or route or anything
  - Simple solution?
- Growing **virtual** pair trees

Specctra prep school Content

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- Pre routes ??
- “2 grid or not 2 grid, why is the question”
- Dog food for fat dogs
- Test points sooner or later or never
- Avoid Silkscreen & silly escapes.
- Power
- Delay delay rules to till last
- What do I know about version 15.0 ?

CONNECTOR OK IN 14.1 NOT IN 14.2 YES 15.O

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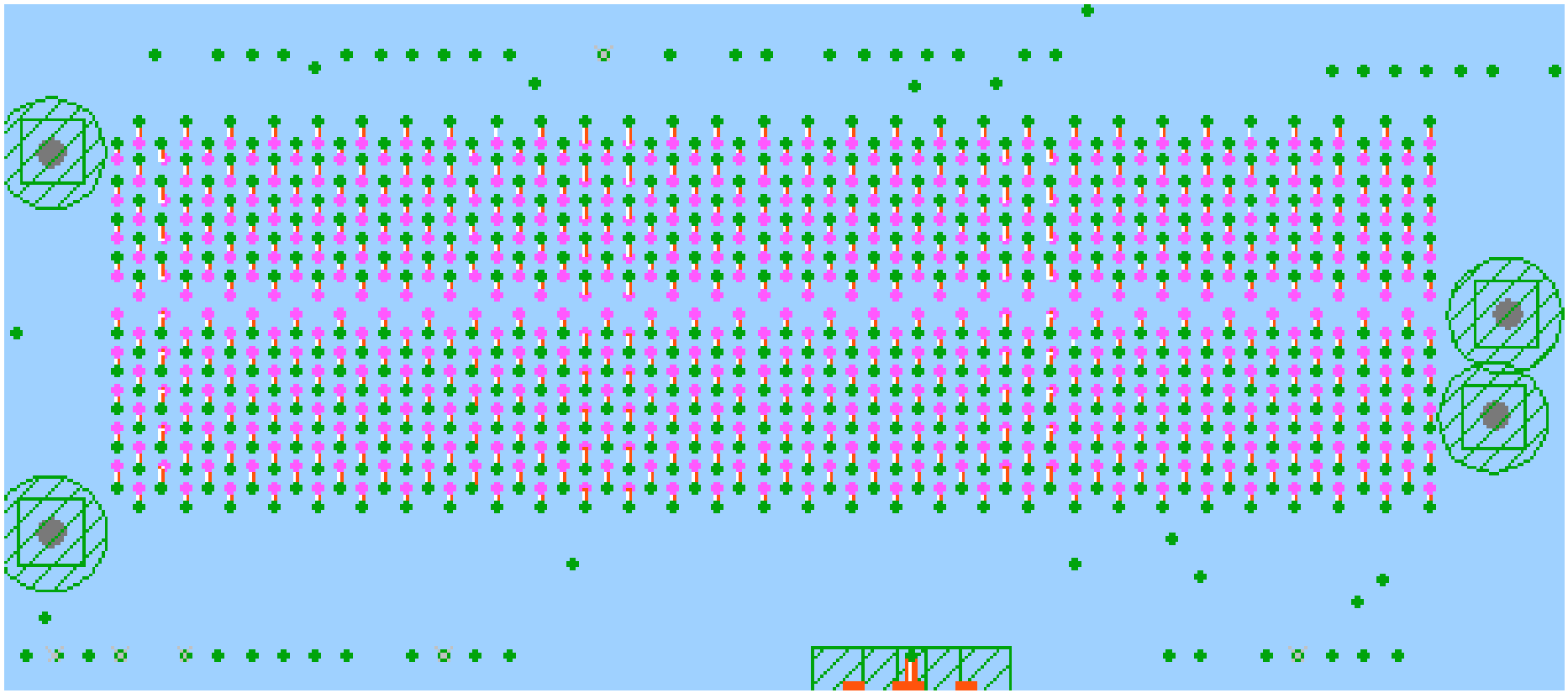
- NEXLEV CONNECTOR 600 pin mother to daughter



CONNECTOR OK IN 14.1 NOT IN 14.2 →15.O OK

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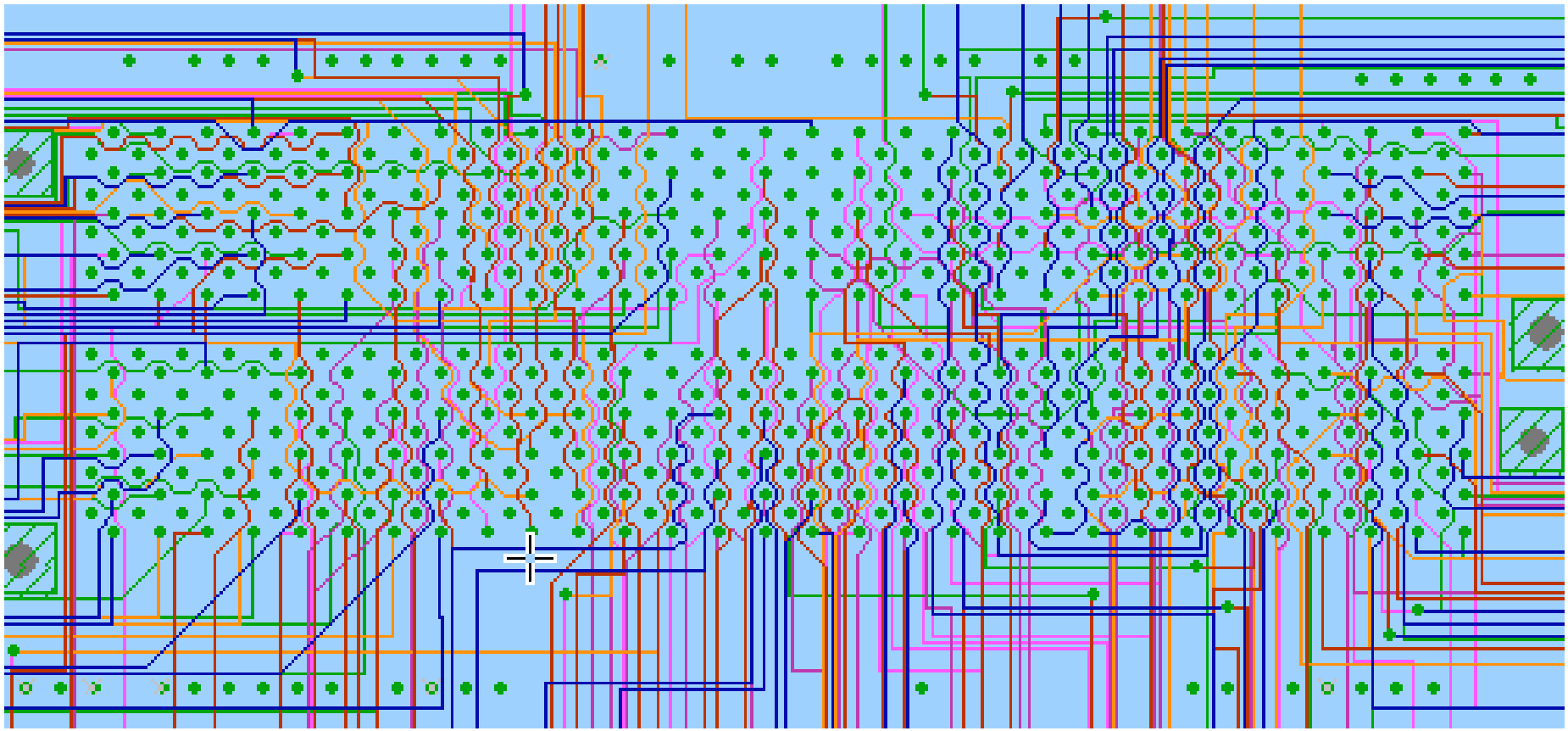
- NEXLEV OK IN 14.1 AND 15.0 100% 2 minutes



CONNECTOR OK IN 14.1 NOT IN 14.2 →15.O OK

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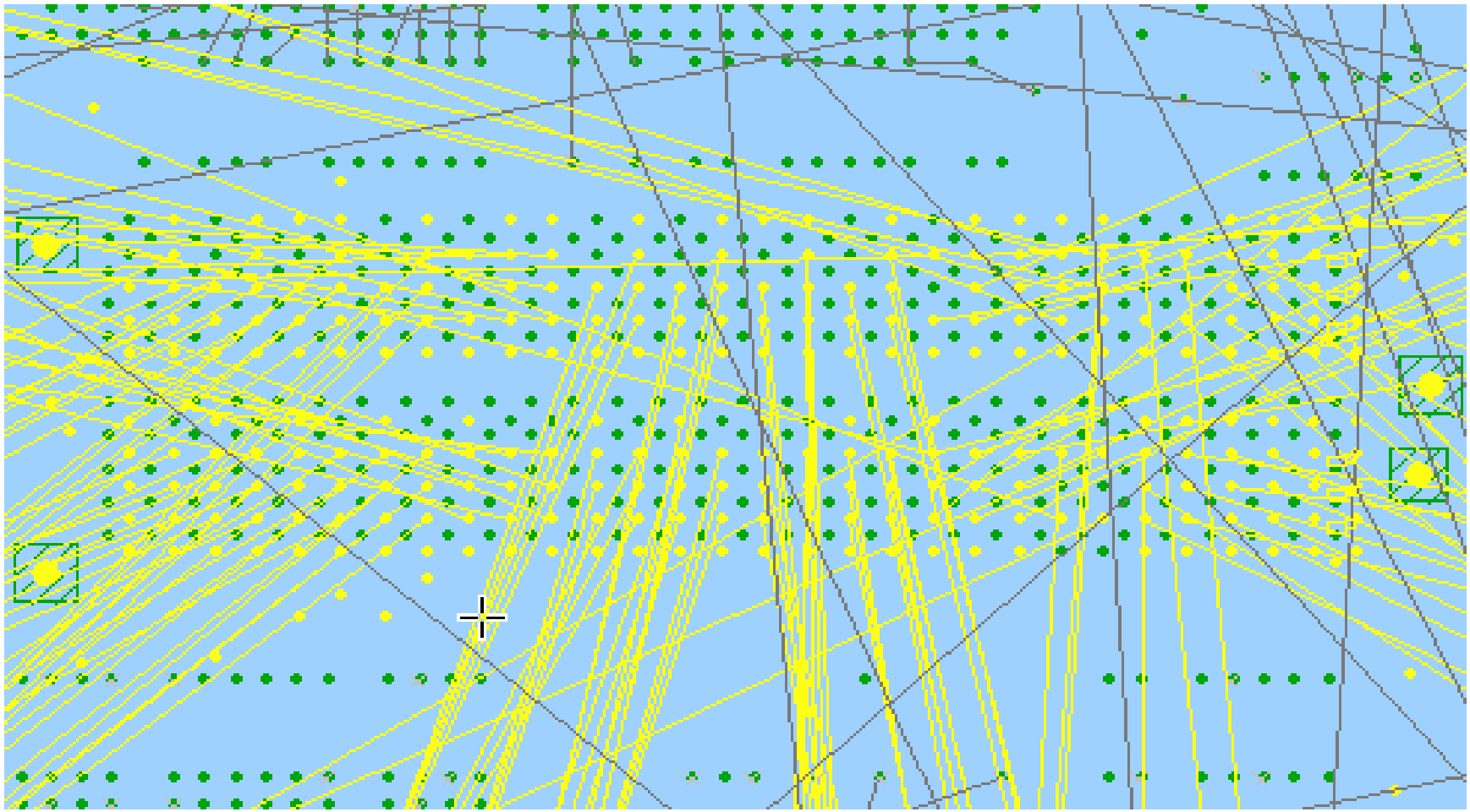
- NEXLEV in 14.2 auto fails will route manual



CONNECTOR OK IN 14.1 NOT IN 14.2 →15.O OK

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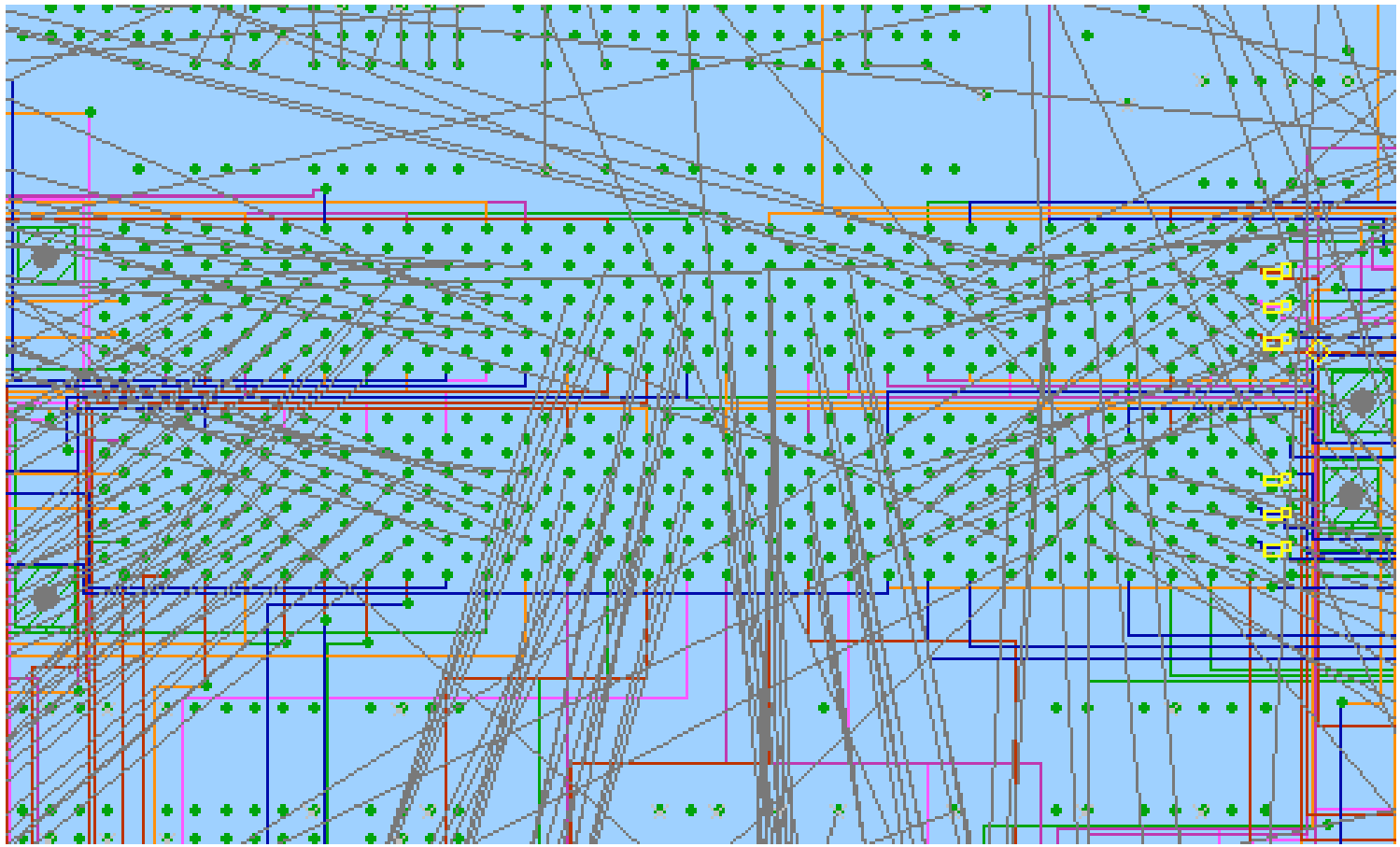
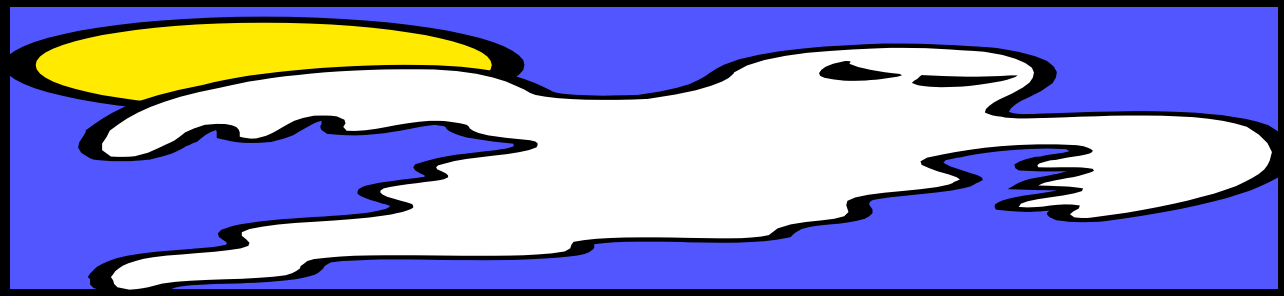
- NEXLEV in 14.2 auto fails





- Isolating root cause on complex design with many problems in addition to this not easy.
- Some of the tag team in 14.1 some in 14.2 (gone yesterday back today) COULDN'T -> 14.0
- The progressive hook it up first methodology eventually got us back to sanity
- Could not continue in 14.1 -- needed the 14.2 separated rule do file to survive.
- 14.1 gen. dsn OK in Specctra 10.1 or 10.2
- 14.2 gen. dsn NOT in Specctra 10.1 or 10.2
- DAYS LOST -> spif -> workaround in 14.2

CONNECT it NOT IN 14.2 EXORCISMS

- If design does NOT have constraints built in then -> export 14.0 and generate dsn in 14.1 (if you have access to 14.1)&(if export 14.0 works)
- We did several this (ABOVE) way
- OTHERWISE TEXT EDIT (SECRET POTION) 14.2 DSN
- Careful comparison of the 14.1 .dsn with the 14.2 dsn showed the only difference to be the connector fanout via padstack definition.

CONNECTED NOT IN 14.2 EXORCISMS

- In 14.1 dsn the syntax for the via used in the connector via array is:(padstack BGA24C_13SRT
- (shape (circle TOP 24 0 0))
- (shape (circle PWR1 24 0 0))
- (shape (circle GND1 24 0 0))
- (shape (circle SIG1 24 0 0))
- (shape (circle SIG2 24 0 0))
- --------etc-(shape (circle BOTTOM 24 0 0)))
- In 14.2 dsn the syntax for the via used in the connector via array is: (padstack BGA24C_13SRT
- (shape (circle signal 24 0 0))) (That's all!)

CONNECT IT NOT IN 14.2 EXORCISMS

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- That this padstack syntax has this impact on Specctra auto routing is right out of Ripley's.
- Transplanting the 14.1 padstack syntax in the 14.2 dsn makes Specctra 10.1/2 work.
- Specctra 15.0 will accept the 14.2 (2 line) syntax and Allegro 15 spif generates the 2 line syntax which works in Specctra 15.0
- Specctra 15.0 routes to just hook up the connector completely 25% faster than 10.1
- 25% is not general but about 10% is my overall average estimate based on several benchmarks.

Strange Bends and flow disruption surprise

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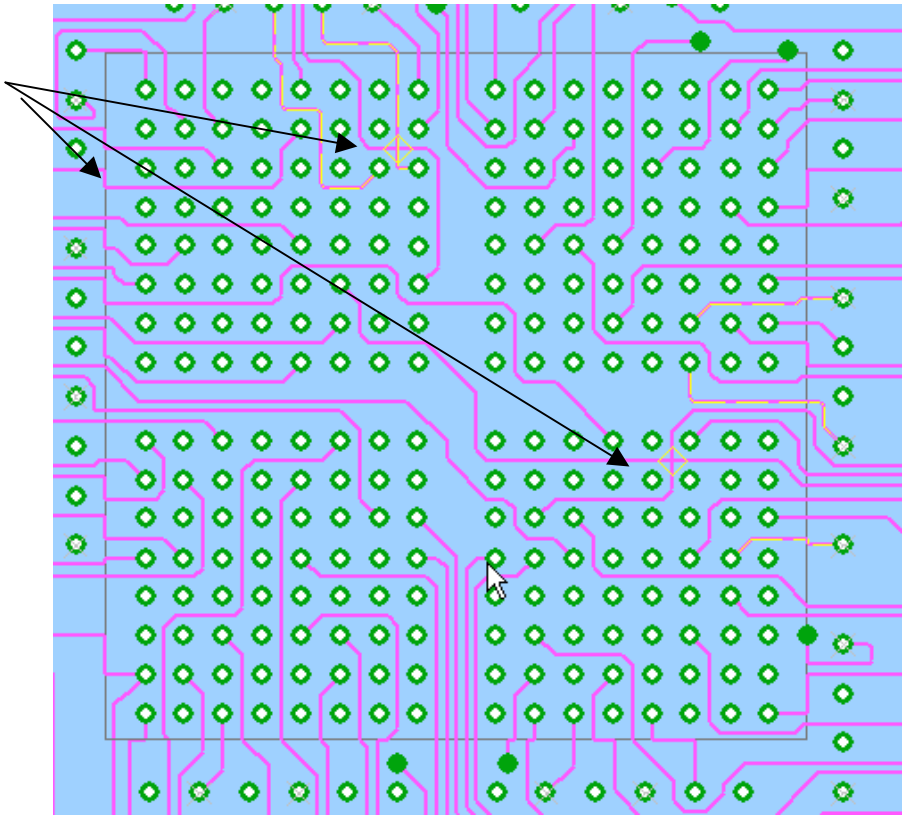
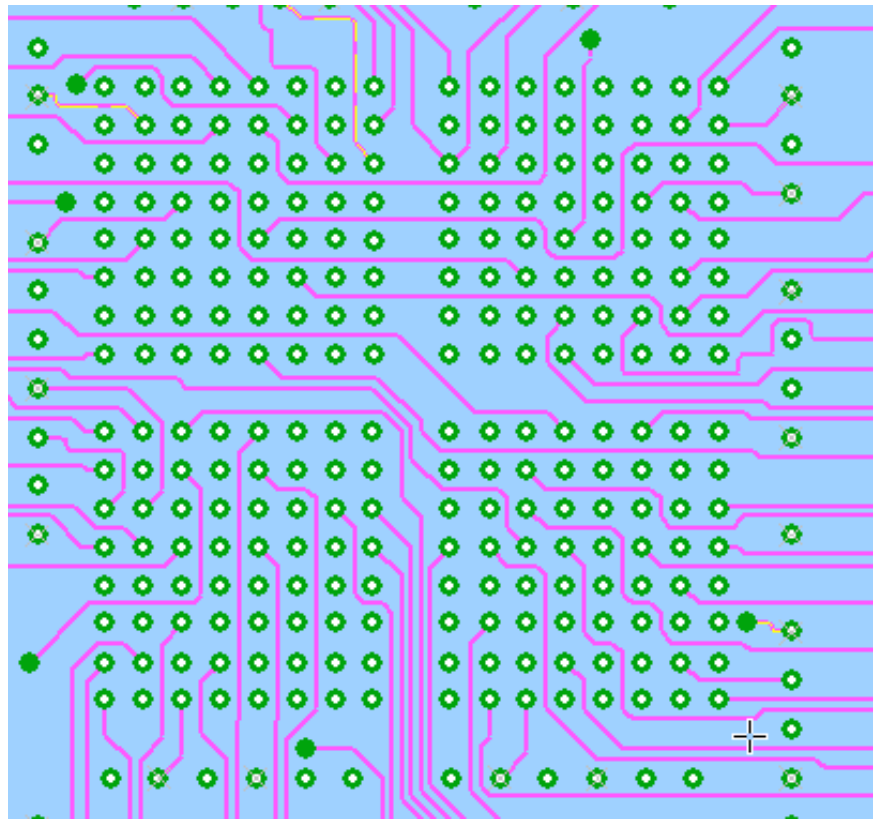
- Accidental regions degrade routing, miter, and trombones!





Strange Bends and flow disruption surprise

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- Regions can be useful but must be carefully managed
  - All rule areas defined in Allegro for whatever purpose migrate into Specctra as regions often on all layers.
  - If no special clearance rules are defined they inherit the lower priority rules and disrupt things for no good reason.
  - The boundary of a region creates a new segment for each trace that crosses it – one for the rules inside and another for the rules outside.
  - Routing flow, miter processing and tromboning are disrupted.

Region control

- Make sure all regions that do not have a specific routing purpose in Specctra are deleted.

- Make sure that required regions are ONLY present on the layers that need them. Example a bga requires special smd to via or through hole via to via clearance

  - ONLY a region on the top layer is required for smd clearance.
  - And then only if the fanouts are being done in Specctra.
  - If done in Allegro fanouts are protected in Specctra so the region is not needed unless we expect specctra to utilize vacant via sites in the via array. (a useful case)

Region control

- If we have a set of diff pairs that require a clearance reduction in a bga via array.
  - If the pairs are constrained to only certain layers then the regions are only required on those layers and in some cases only in some quadrants of the bga via array.

- A similar technique can be applied to multi row connectors with the bonus of providing guidance by limiting the region definition to avoid wandering around unnecessarily.

- Watch out for Specctra using regions to cheat on wide trace power. Job for region class rule.

Region control

- On very congested designs it sometimes is necessary to define temporary clearance rules that will allow access to the bga via array for the hook up stage in the auto routing.

- Later once Specctra has found the hook up bga channels with crosses/clearances down, regions rules are defined and clearance rules redefined and routing continues.

- Avoid using a temp width in this way because Specctra will not necessarily change width with a rule change and has no check for width violations.

Region Improvements

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- The level of disruption seems to have improved a bit over the last few revisions.
- Performance benchmark of specctra routing a region in 10.2 and then in 15.0 showed a 20% run time reduction on this design on this day. 1:21 -> 1:00
- The addition of region net rules, region class rules and region class_class rules provides solutions to some tricky problems like the power one, and high voltage special clearances that regions on their own messed up on.

Region has a new use in version 15.0

- We will have Specctra popping vias through small planes on the signal layers & plowing into these planes with traces!
- How to keep the Swiss cheese from becoming all hole and no cheese? And cut up in unconnected strips?
- Defining a region with brutal clearance via to via, wire max stagger, region class_class wire to wire will help avoid “all hole and no cheese.”
- We really do need an additional set of clearance rules for for poly wires (WYSIWYG planes)!

SLOW

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- VERY DENSE HEAVILY CONSTRAINED DESIGN:
  - 4” X 8” Area/EIC= 0.049 sq. in
  - Components=2052 SMDs=1915 Pin Count: 10483
  - Start vias **15106 (micro and buried)**
  - MICRO VIAS IN PAD OR TANGENTIAL FOR almost ALL DEVICES TOP AND BOTTON.
  - TO ALLOW tight OUTSIDE PLANES FOR EMI SHIELDING.
  - TO ALLOW NON MIRRORED BGA’S OVER AND UNDER ALSO BGAS OVER FPQ’S and lots of discretes

SLOWER

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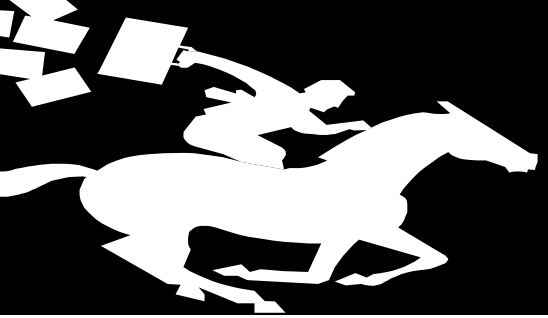
- VERY DENSE HEAVILY CONSTRAINED DESIGN:
  - 320 nets in 160 diff pairs use layer, via limited to escape only, topology length specified.
  - Single ended topology length matched sets, layer control.
  - 24-7, 3 and later 6 player tag teams parallel Specctra effort
  - During early feasibility experimental placement stage of routing Specctra running just fine on **1.8 Gig** machine
  - 10 sec.for dsn load 1 sec. check (type routing) and 5 min for early routing passes dropping reasonably. (ETA 25 -30 hrs)

- VERY DENSE HEAVILY CONSTRAINED DESIGN:
  - Then a couple of updates the dsn load dragged out, check (type routing) 2 minutes then 5 min. then 8 minutes with the first routing to 21 minutes (fanout pass taking 32 min).
  - With this 8 minutes would be the lowest pass time possible for the full run expected to be 450 passes averaging 20 min each.
  - 9000 min -> 150 hours -> 4 or 5 days estimated run time **obviously unacceptable**.
  - Checked positive plane impact and for duplicated shapes. Not the problem!
  - Solution?



-simple

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- VERY DENSE HEAVILY CONSTRAINED DESIGN:
  - In startup menu -> more options , click **simplify polygons**
  - Or on command line add option **–simple**
- On this design speed up by **8 to 10 times**
- Able to load the design on 0.5 gig unix machines in finite time. (not infinite time)
- Only works on designs with some  shape problems.
- We made the ETA OF 32 hours!

SIMPLE
PIECE OF CAKE

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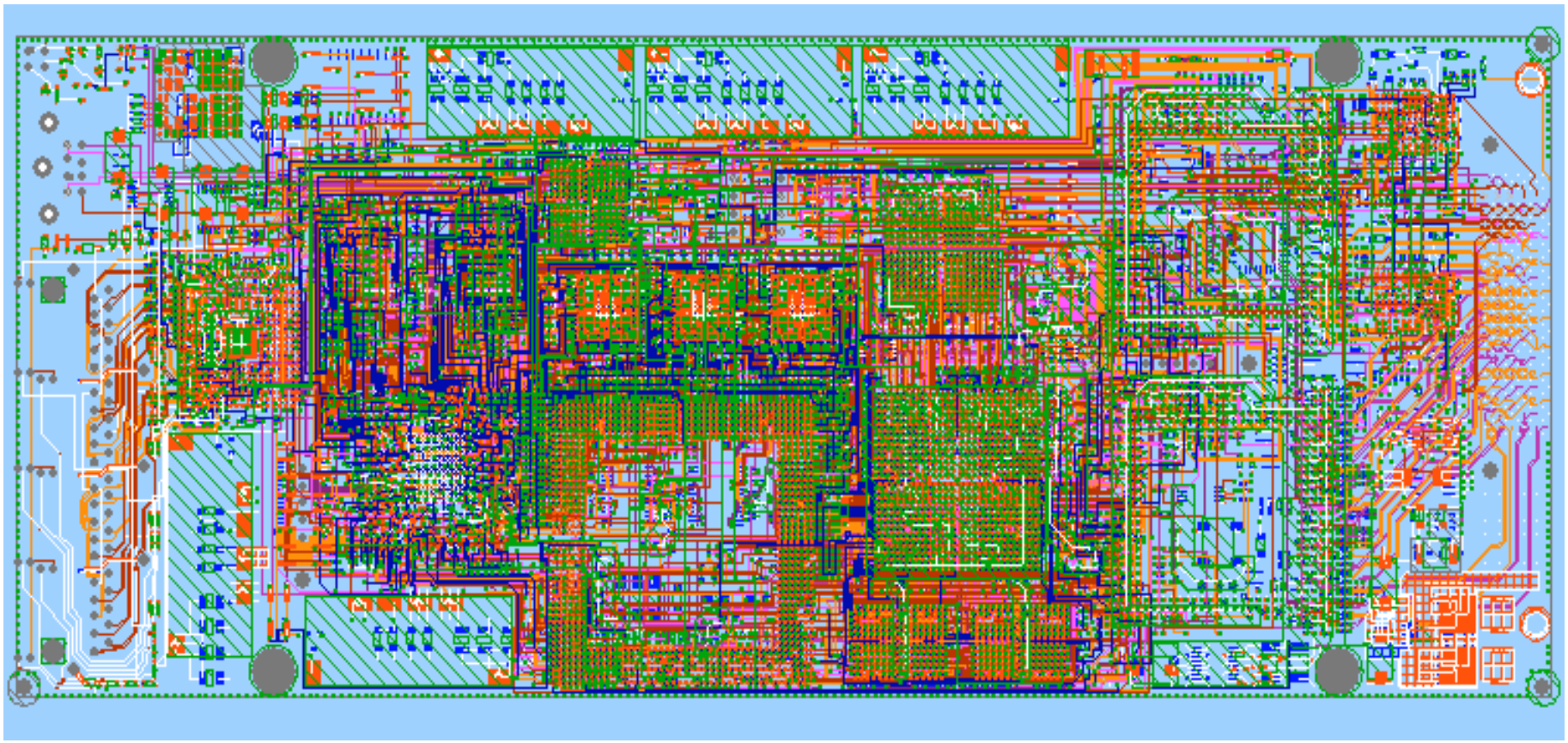
- 18 layer Area/EIC= 0.049 sq.in



SIMPLE PIECE OF CAKE

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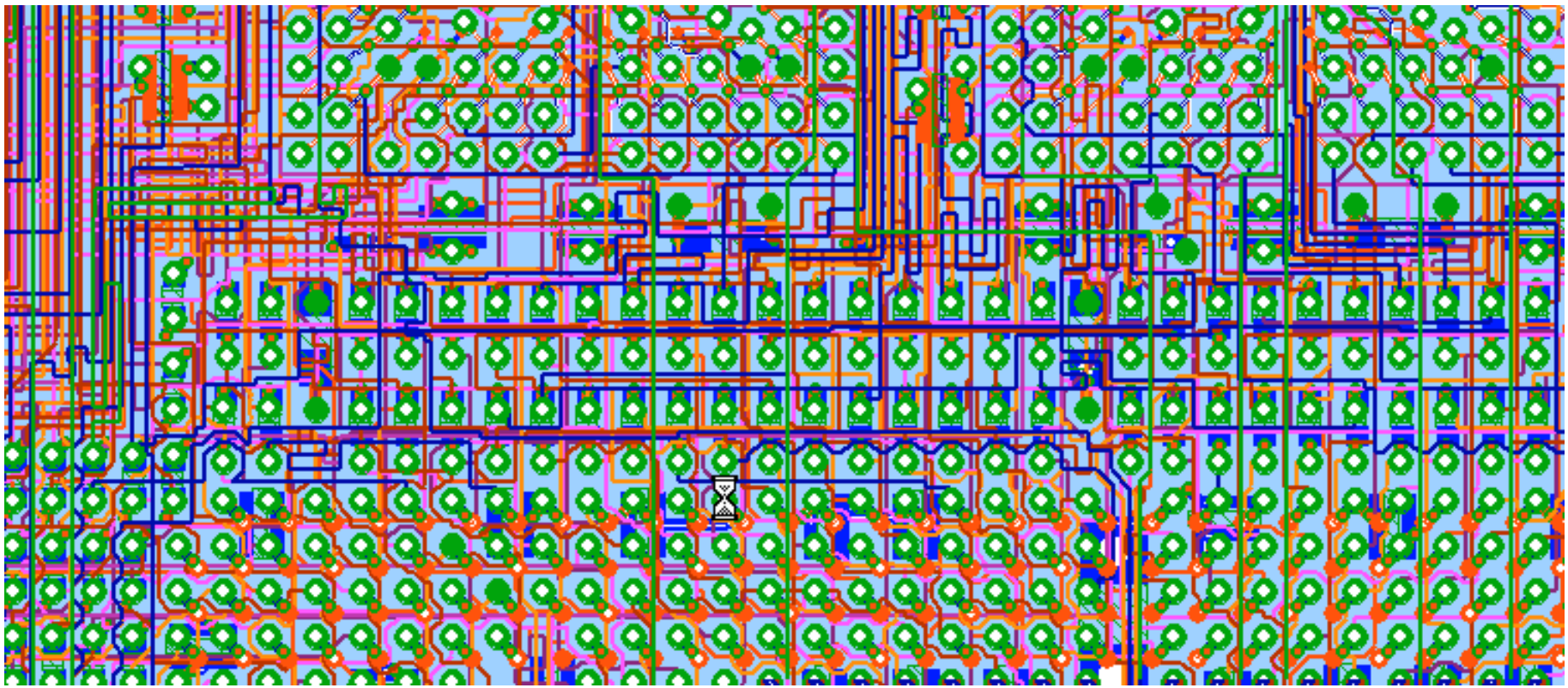
- That's why they are called micro vias



SIMPLE
PIECE OF CAKE

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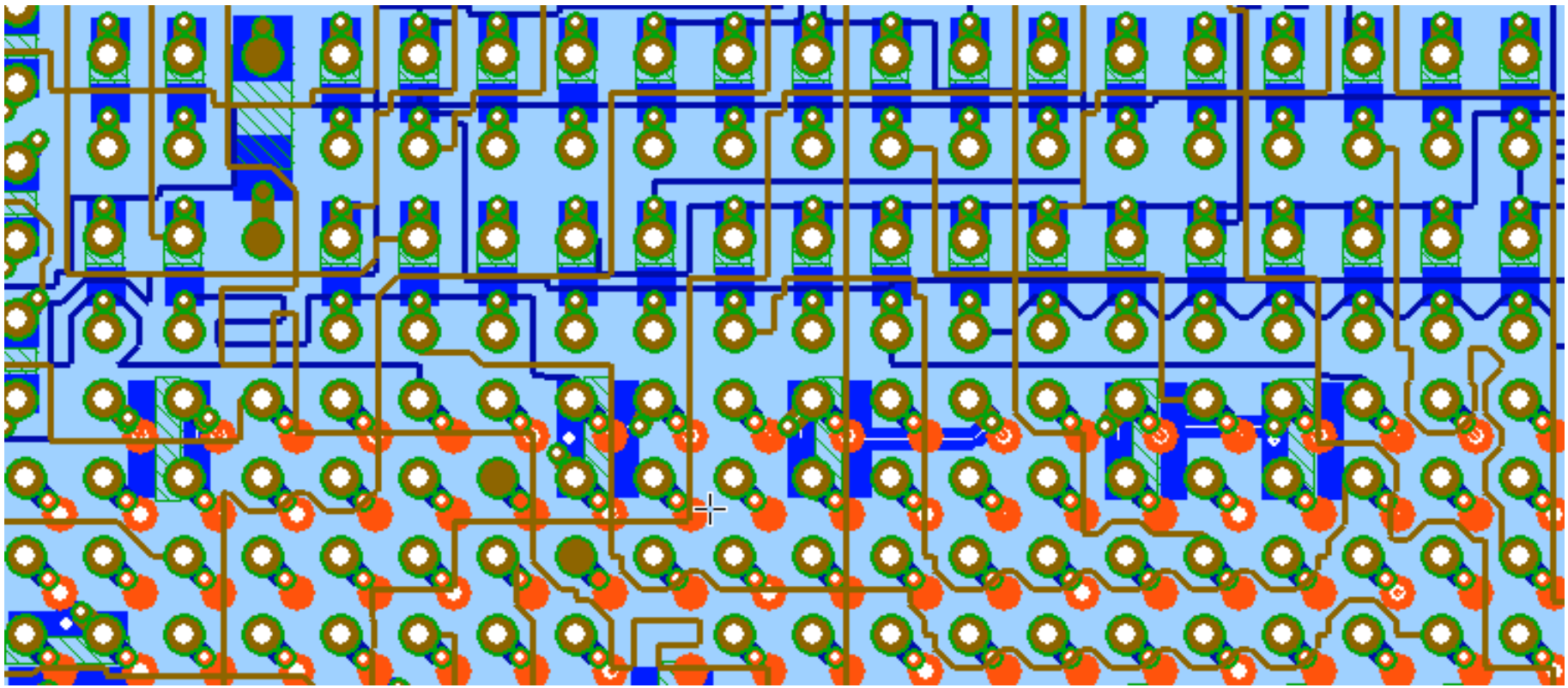
- Neither in nor out (Like a car -- its all in the front end **alignment**)



Perspective
2001 > 2002 > 2003

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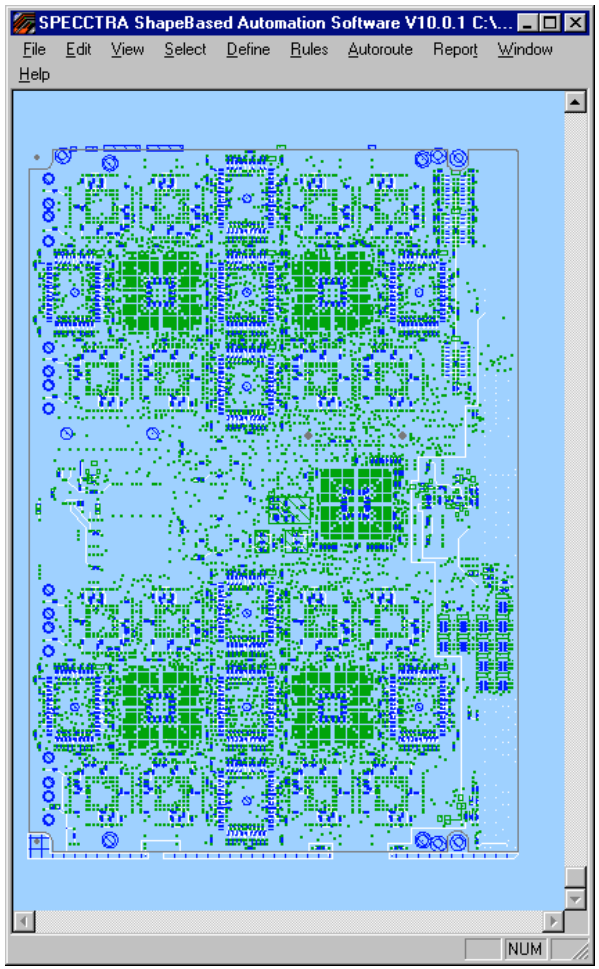

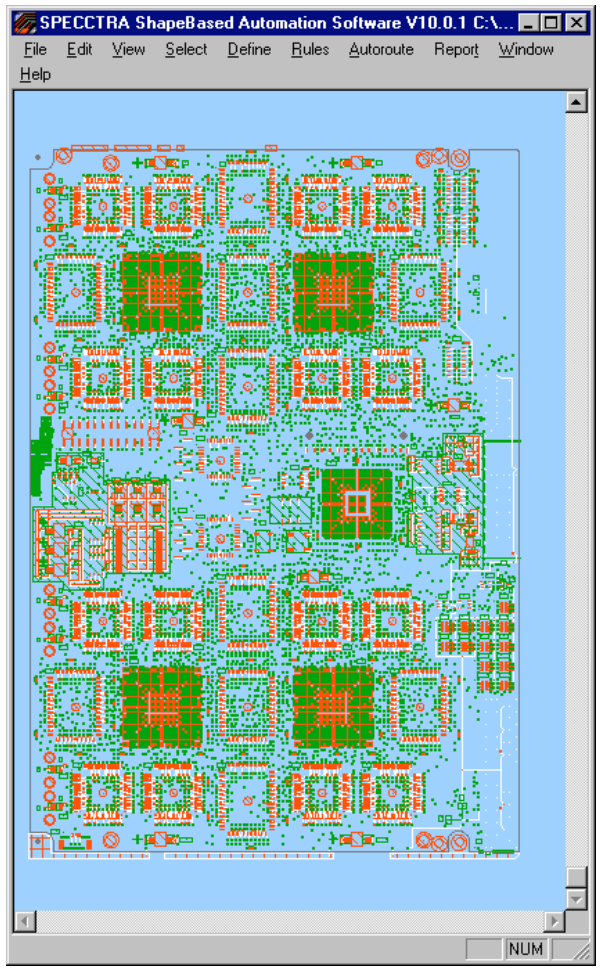

Perspective
2001 > 2002 > 2003

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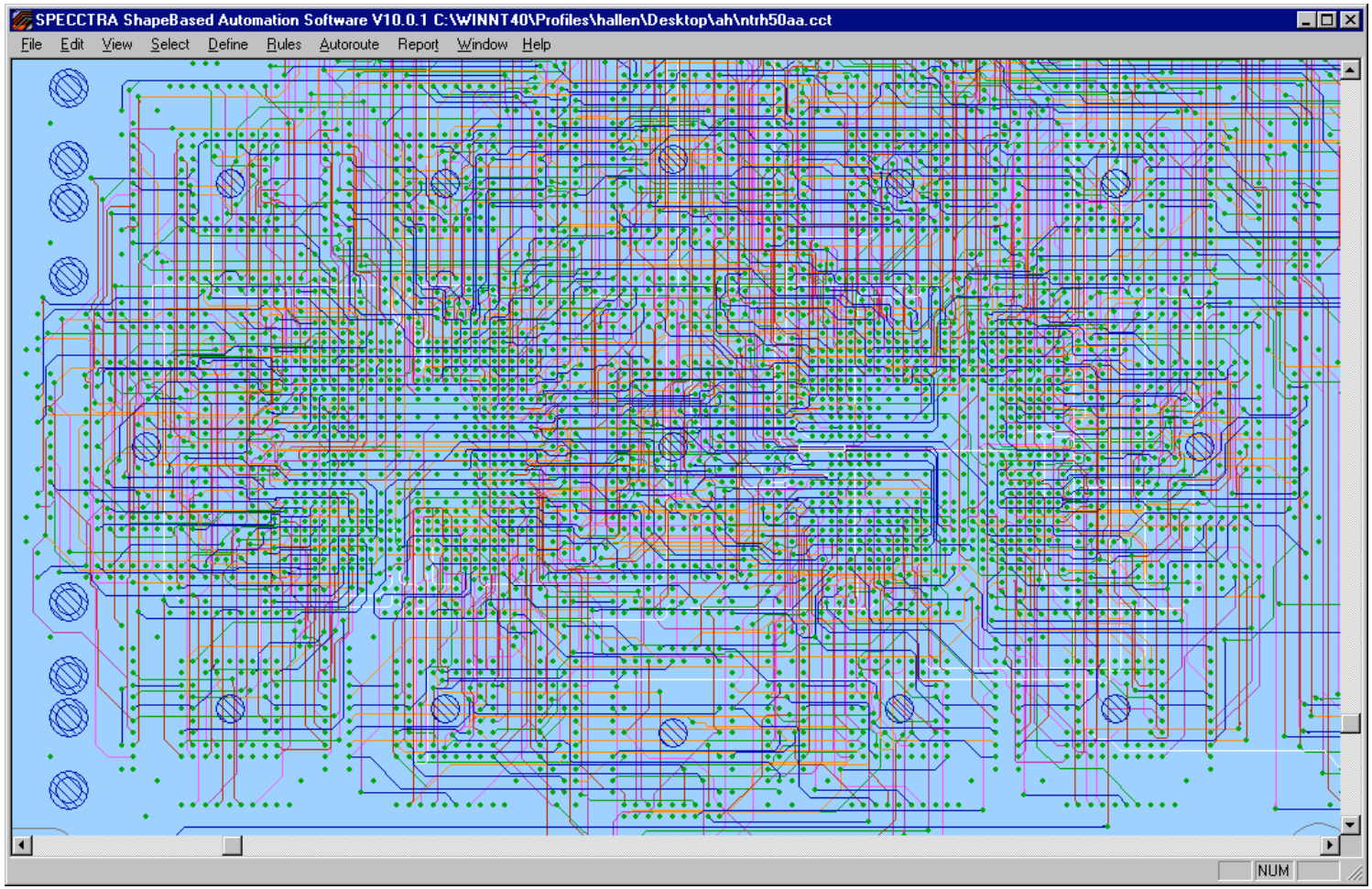

Perspective
2001 > 2002 > 2003

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- THAT BOARD WAS ROUTED IN 2001
- FPQ's back to back with BGA'S over DISCRETES
- `Area/EIC = 0.083 sq.in`
- Routed length= 3903.073
- On machine in use
- 2001 (unix HP 550 meg) routing time 12:51:30
- 2002 (pc 1.8 gig) routing time 8:34:20
- 2003 (pc 3.06 gig) routing time 3:51:27
- SPECCTRA PEFORMANCE IMPROVED SLIGHTLY MACHINE SPEED SIGNIFICANTLY

What We had to do
2001 > 2003 (the "simple" 1)

2001		2003
FPQ's over FPQ's	->	BGA'S over BGA'S
BGA'S over DISCRETES	->	BGA'S over FPQ's
Area/EIC 0.083 sq.in	->	0.049
Nets constrained 40%	->	80%
Run time 13 hrs .5G	->	32 hours 3G
Total vias 8631	->	15894 (900 routing)
Connections 6297	->	7253
Thru hole vias	->	micro in? pad + buried
No manual cleanup	->	6 guy || tag team 3 days

Pre routes
HERE OR THERE ??

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- **Avoid anticipating what will cause trouble in Specctra**
  - **I am often pleasantly surprised at how well it does with something I expected it to struggle with.**
  - **I am sometimes quite disappointed when it flounders on something I thought should be easy.**
- **For things that just must be pre routes such as:**
  - **the customer insists (Rule #1 CIAR).**
  - **Extensive specific via sharing in BGA'S and discretes**
  - **Specific but not all BGA unused pins need no via**
  - **Pair fanouts should not throw off the skew before we start**

Pre routes
HERE OR THERE ??

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- **TAKE THE DESIGN INTO SPECCTRA AND DEFINE THE CLASS/RULES FOR THE SETS OF “manual” NETS.**

- **GIVE THE AUTO ROUTER A SHOT AT JUST THEM ON THE EMPTY BOARD AND YOURSELF AN OPTION**

  a) Clean them up, write them only out in a wire file using the (type select) option on the write wire file and then protect them (they are manual pre_routes and should be as good as ->)

  b) Trash all or some of them and route interactively, then write etc. as above.

Pre routes
HERE OR THERE ??

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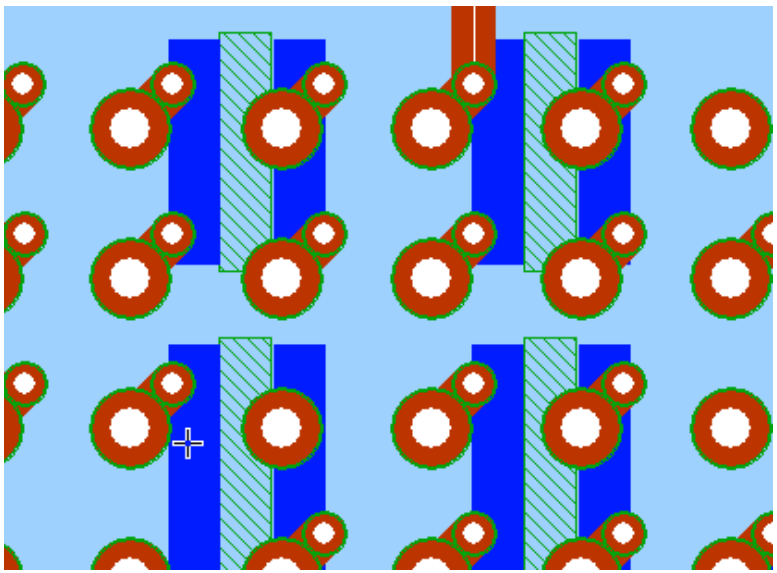
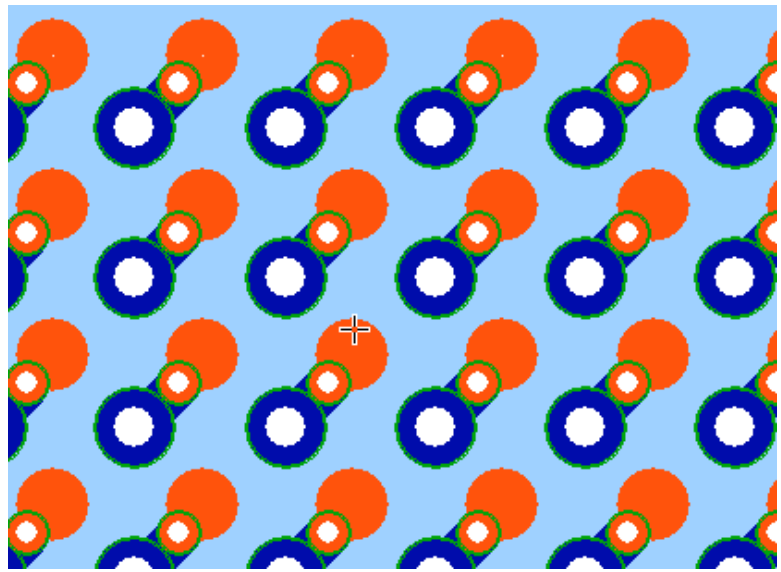
- **The latest monkey wrench the Signal integrity folks have added to the works: Rule #1 (CIAR)**
  - **Multiple fanout vias per pin on discretes particularly, those associated with BGA'S USING MICRO VIAS**





Pre routes
HERE OR THERE ??

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- **What pre route "do" in Specctra "do's":**
  - **After the auto router runs a while pre route stone walls and bottle necks can be seen.**
  - **Pairs often have to be handled as semi pre routes i.e.. Auto route them first cleanup a bit and protect for main route. Keep a wire file pairs only, so you will not need it.**
  - **Pair adjustments become obvious during the auto route**
  - **Certain pre route via unsuitable spacing is causing wide trace and pair access problems.**
- **Make sure pre routes abide by layer bias.**

Pre routes
HERE IS SPECCTRA?

- **Fixing it up during the Specctra auto run:**
  1. **Pause, figure out exactly where you are in the do file.**
  2. **Stop Specctra , determine what is currently selected, then unprotect class manual_routes**
  3. **Make the required changes to the “pre routes”. in the presence of the problems they are causing**
  4. **unselect all, select class manual_routes, write a wire file (type select), unselect all, PROTECT class MANUAL_routes.**
  5. **Reselect whatever was selected when stopped, paste the balance of the do file into a continue.do and execute.**

Pre routes
HERE IS in SPECCTRA!

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- **ADVANTAGES OF HERE BEING in SPECCTRA:**

  1. **You can often do it in less time than my description.**

  2. **Definitely faster than going back to Allegro to fix then reloading .dsn and restarting main.do from the beginning.**

  3. **If pre route rule changes have to be made, just make sure to change them in their source.**

Pre routes
HERE IS SPECCTRA!

- **ADVANTAGES OF HERE BEING SPECCTRA (cont.):**

  4. **The required changes to the “pre routes” are made in the presence of the problems they are causing**

  5. **The wires are saved, if later, a net list change or required placement change comes through the time to adjust is minimal as the pre routes are read in and adjusted at the beginning of the change.**

- **Something to think about.**

2 grid or not 2 grid
WHY IS THE QUESTION

- **Remember a long time ago, all you had to do was GET THE GRIDS RIGHT.**
  - If you really got **GRIDS** absolutely right the world was **WONDERFULLY STRAIGHT** forward. (almost boring)
  - **Grids** solved test points, flow, and in the very early CAD days **all spacing requirements and all manner of problems**.
  - Generally designs were ALL mil or ALL mm (pre globalization)
- As the electronics World continued implosion along came:
  - Smd ‘s , mixed mil/mm technology designs, accelerating high speed, and just tons of other interesting stuff.

2 grid or not 2 grid
WHY IS THE QUESTION

- **Along came CCT with Specctra and "Shape based" said to be "gridless".**
  - While it was and is true (almost again) that Specctra is gridless, never the less Specctra just loves coarse grids on designs where they are possible.
  - Recognition by CCT, brought, forth the command "grid smart". It still works well on some designs (mainly respins)
  - That 2001 design was done with course 5 and 25 mil grids -- remember **no cleanup** (shipped to the board shop as it came off the auto router).
  - Isn't that interesting its gridless but it likes grids – I Wonder?

Specctra does not wiggle WELL

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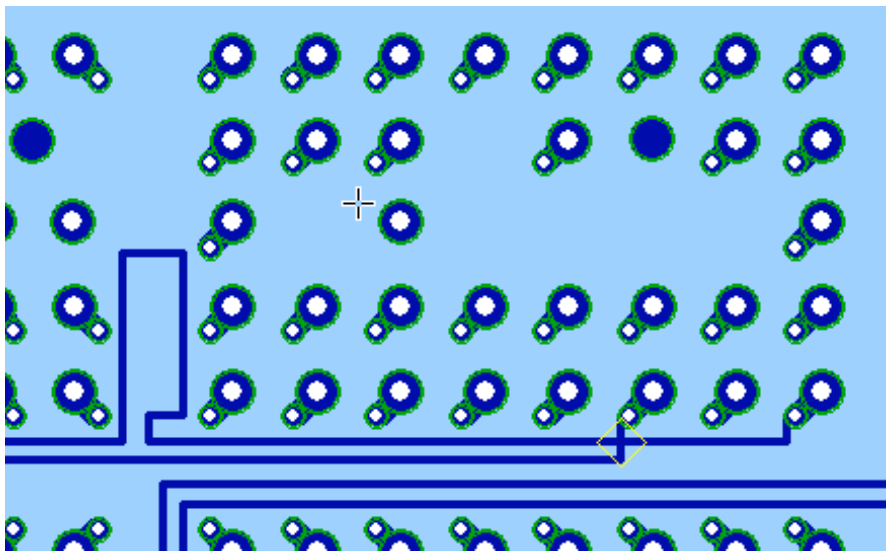
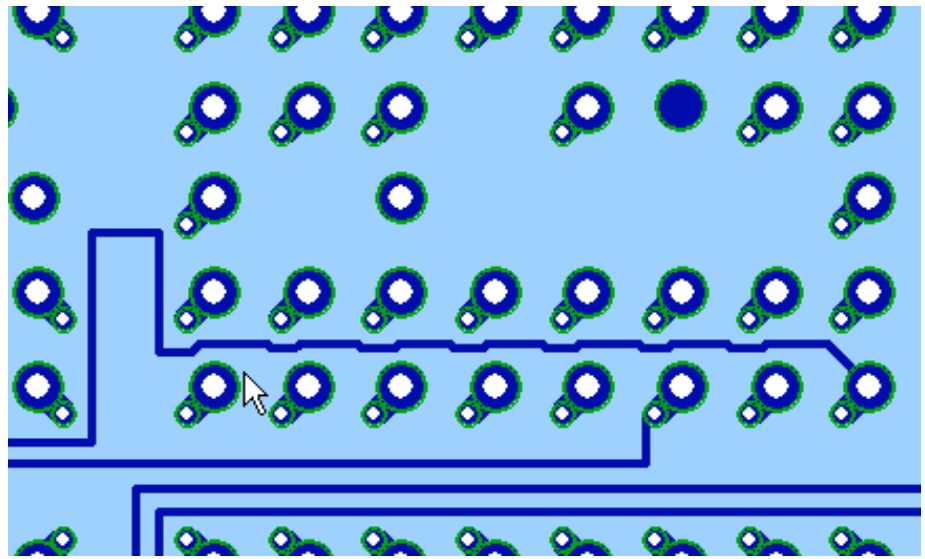
- **This shows up (a) as failing to clear easy shorts that require wiggle to solve and unused channels.**





Specctra does not wiggle WELL

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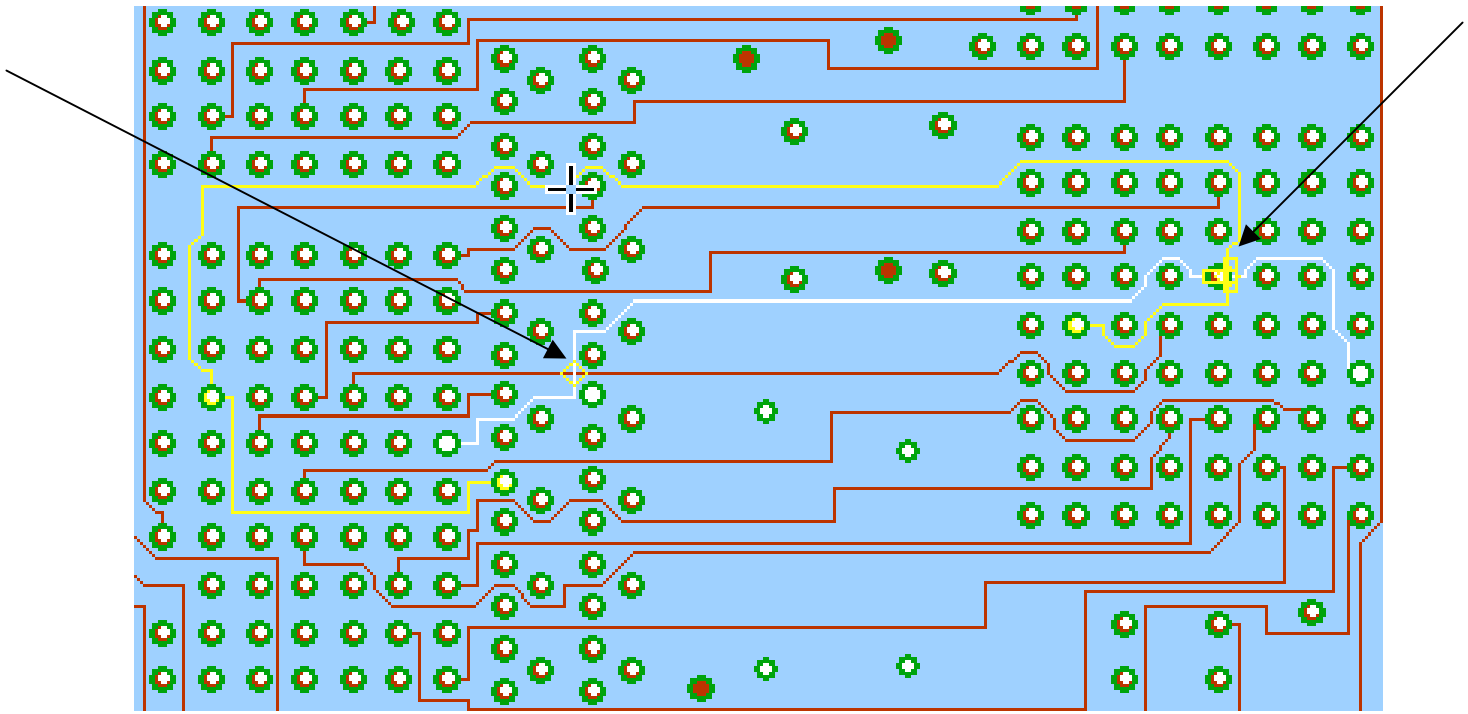
- **This shows up (b) as wiggling with connections and then not finding easy solutions.**



Specctra does not wiggle WELL

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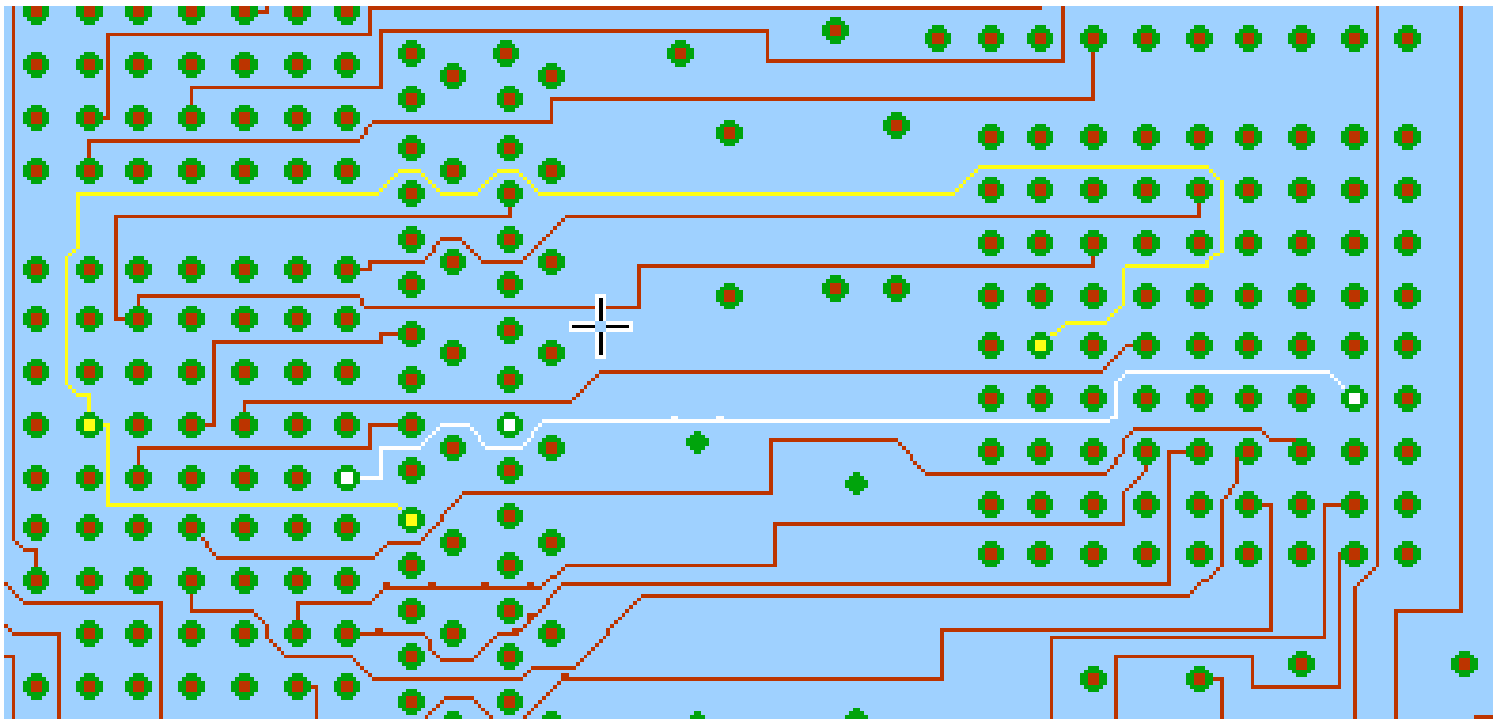
- **This shows up (b) as wiggling with connections and then not finding easy solutions. (easy interactive)**



Specctra does WIGGLE a LOT then HIDES IT

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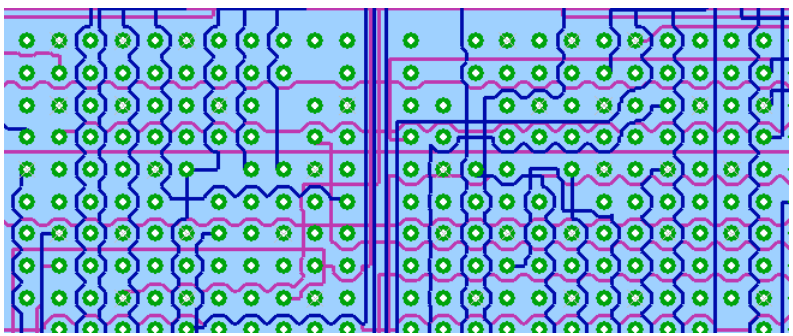
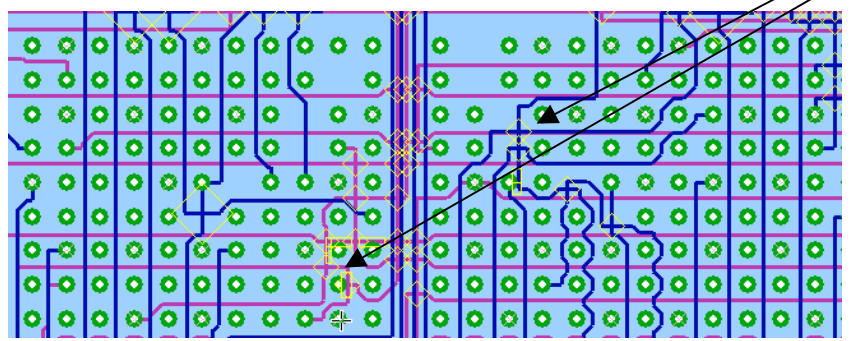
- # 422 bend points have been removed.
- # 546 bend points have been removed.
  - Ever notice those remarks at end of each pass?
  - It cleans up those that are violation free ok
  - But ones that will have be worked on in the next pass (conflicts) still bent out of shape.
- JUST BEFORE END AFTER END N bends remove





WHAT IS THE POINT OF THIS FOR SPECCTRA PREP ??

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- FOR VIAS THAT WILL BE PROTECTED DURING AUTO ROUTING:
  - ALIGNMENT IS CRITICAL.
  - EFFICIENT SPACING IS CRITICAL.
- WHETHER THE FANOUTS, DOGBONES, MICRO VIAS TO BURIED VIA STEPS ARE DONE IN ALLEGRO OR DONE IN SPECCTRA WITH FANOUT THEN PROTECTED---
  - These are THE DIFFERENCE BETWEEN POSSIBLE AND NOT POSSIBLE ON TODAYS DENSE BOARDS.

FRONT END
ALIGNMENT CRITICAL!

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- **FOR A MM PITCH BGA OR OTHER MM VIA ARRAY SUCH AS LARGE SMD CONNECTORS:**
  - **THE DISCRETES CLUSTED AROUND CLOSE BY, NEED THEIR VIAS IN LINE WITH THE MAIN ARRAY.**

- **For micro vias landing tangentially or partially over lapping the pads of buried vias careful consideration of the dominate required flow for the double pad layers is required or these layers may be little use to the router.**

FRONT END
ALIGNMENT CRITICAL!

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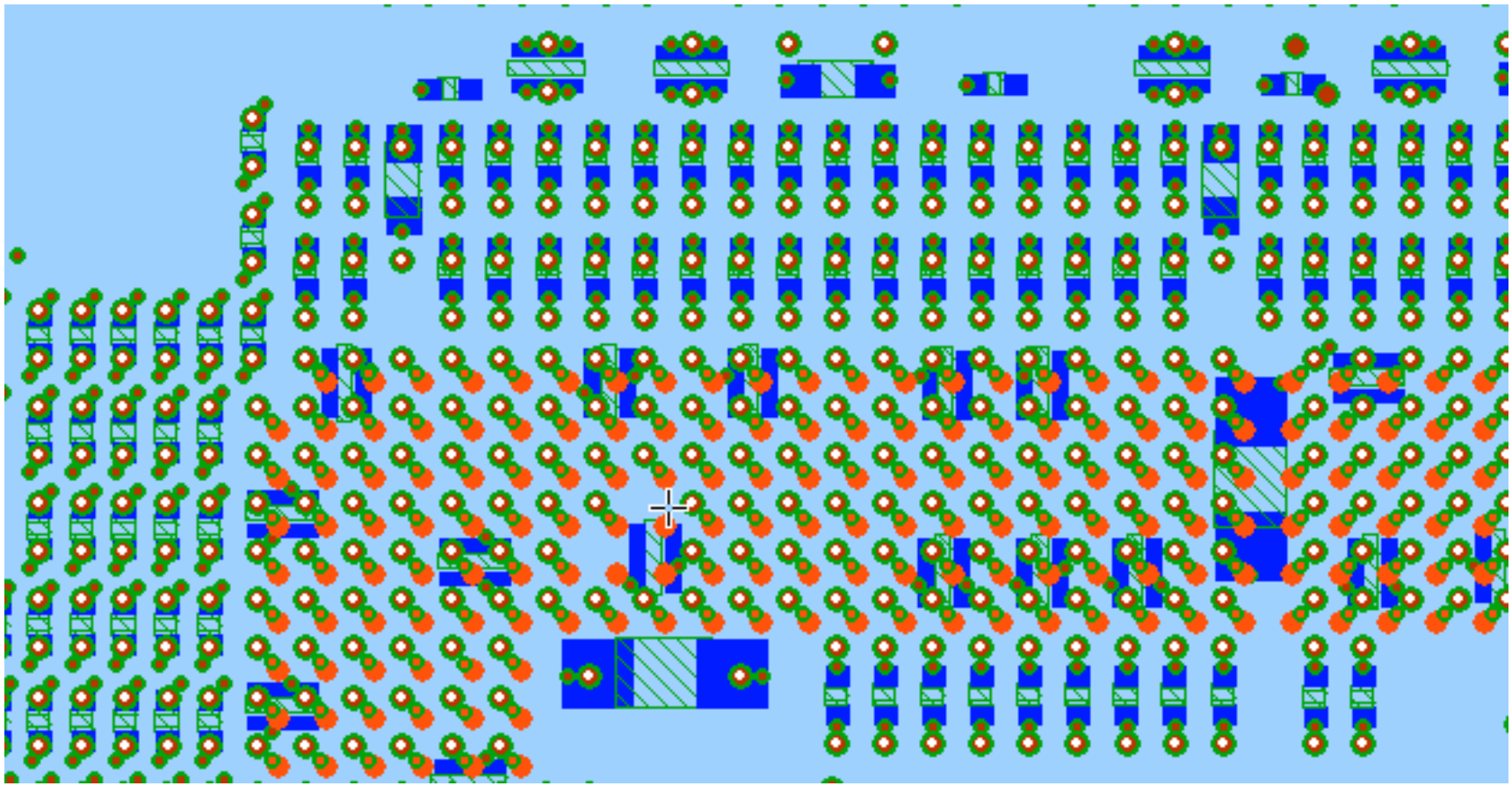

FRONT END
ALIGNMENT CRITICAL!

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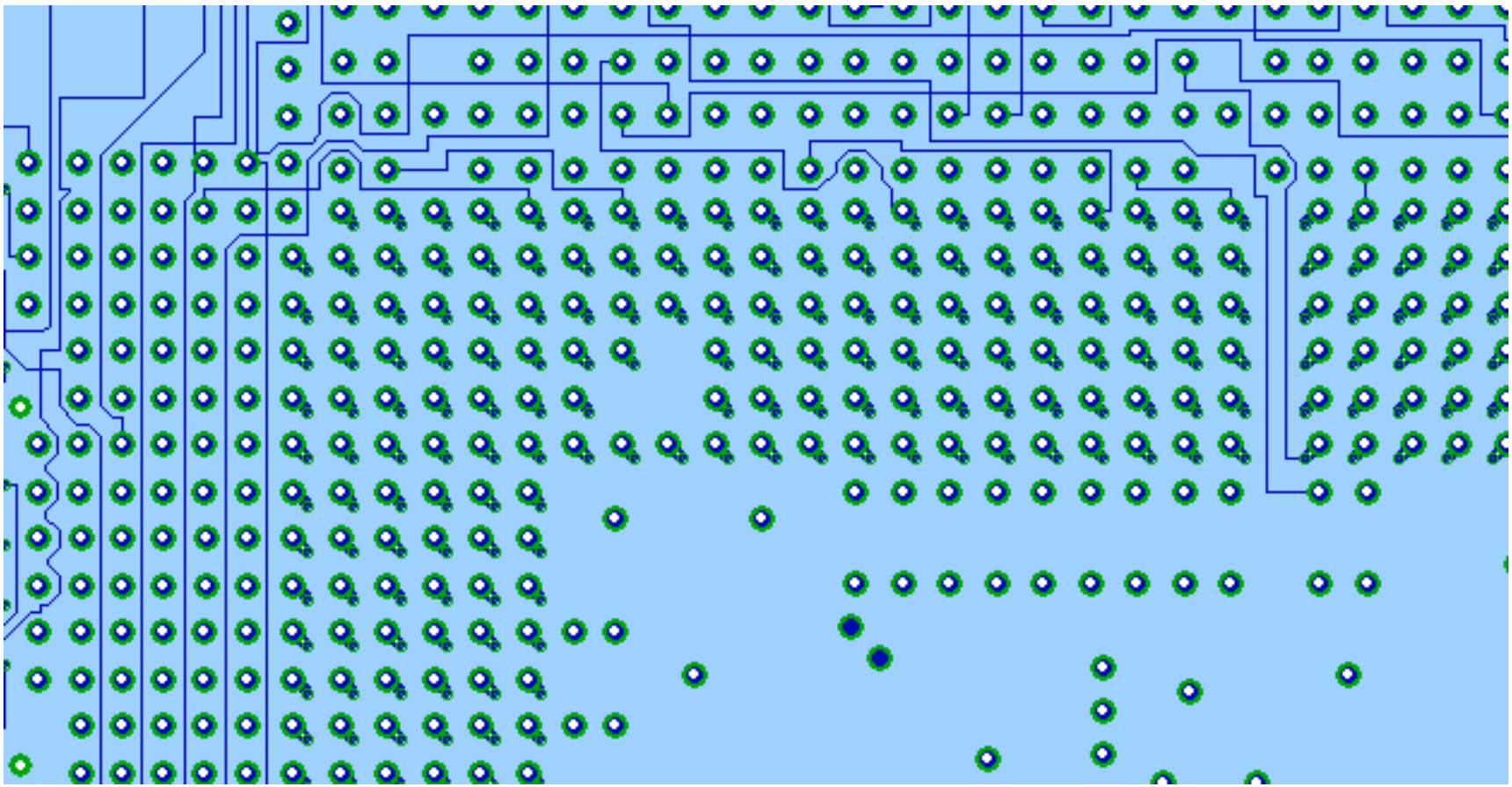

PROTECTED VIA PAD SPACING CRITICAL!

- **In the good old days this was easy 5 mil trace and space, pad to pad via was 15 or 25 -- job done.**
- **Now we have mm and mil pitches with a mix of 4 mil trace 5 mil trace diff pairs with odd gaps 7 mil traces !**
  - **Figuring out the magic numbers for via to via space is not always obvious.**
  - **It is well worth while giving it serious thought.**
- **Having protected pre routes control in Specctra so the auto route run can pause, stop, some via adjustments made where there are problems, & continue is nice.**

Dog food for fat dogs have to diet

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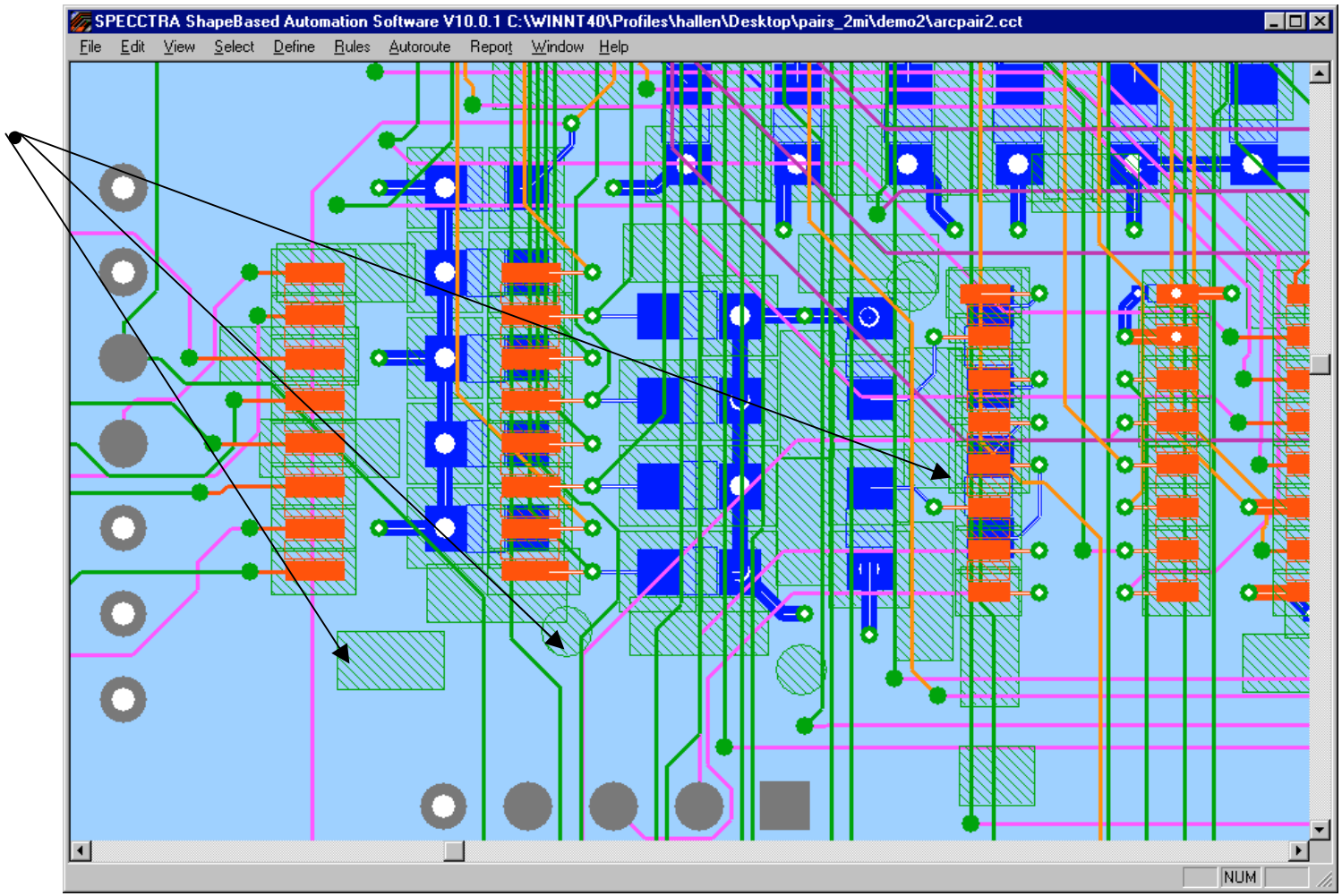
- **BGA'S are the dogs that are getting too fat. We have to reduce the number of dog bones we give them.**
  - **Some single net pins have nothing inside.**
  - **Some unused gates can have shared vias if grounded.**
    - **Great way to reduce test point problems**
  - **Some power or gnd pins can share if we put a mat outside**
  - **Can source pins feeding multiple loads exit to a virtual pin and feed from there?**
  - **Strategically placed micro vias?**
- **Early exploration with the circuit design and SI folks**

PREP SCHOOL
Test points sooner, later, never

- **To avoid "never" or terrible pressure at the end, get a test point plan way back in the placement stage.**
  - **Jtag or other reduction method is not last minute thing.**
  - **Get the circuit and manufacturing folks talking early re:**
    - **Only need test point on 1 side of series resistors?**
    - **Only need TPS on some? None? Of Unused gates?**
    - **Grounding unused gates with shared vias?**
    - **Identify nets that are just too high speed to have TP'S.**
    - **Identify pins with nothing inside**
- **Test point prior to complete fanout or routing!**

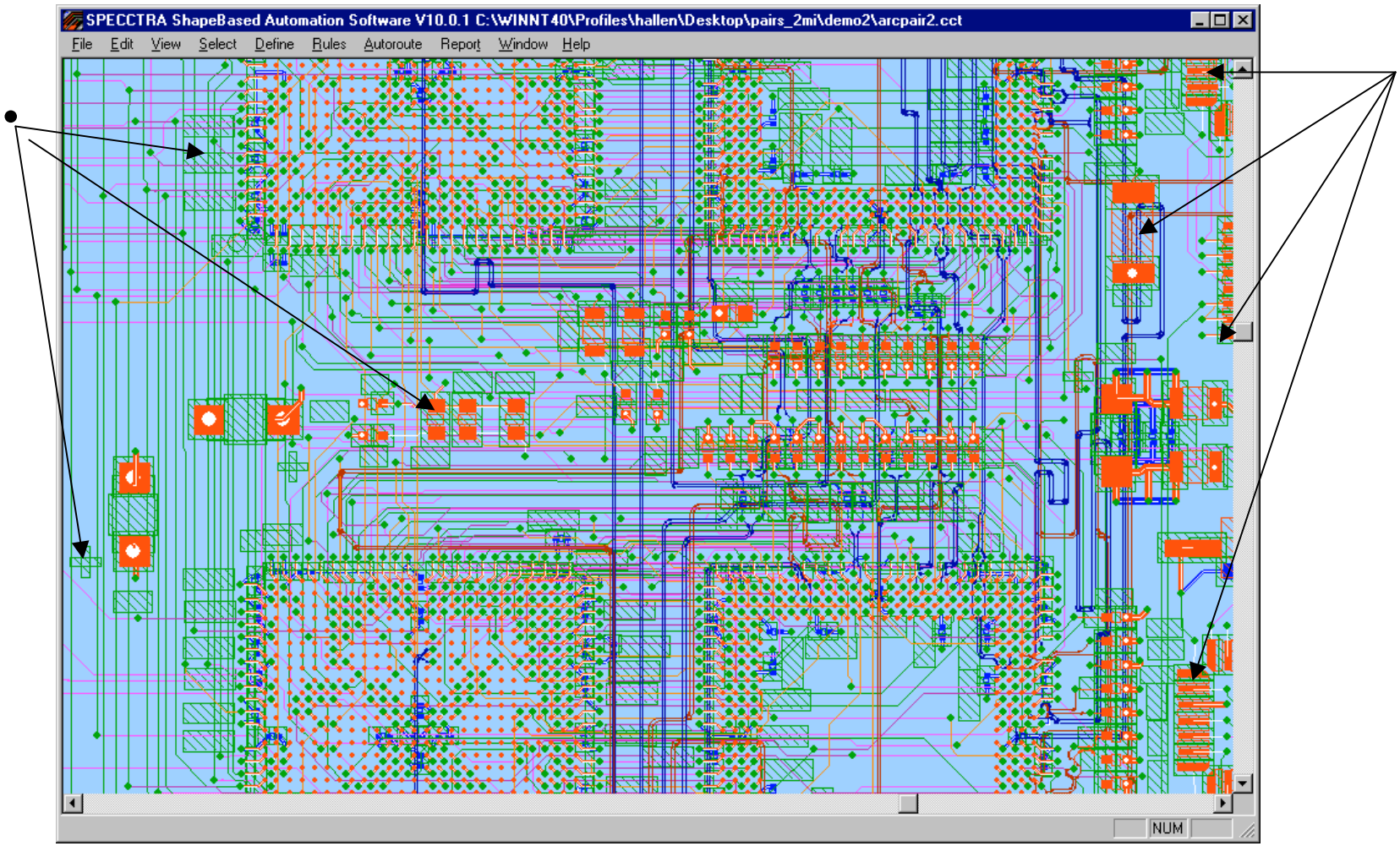
PREP SCHOOL
Avoid Silkscreen & silly escapes

International Cadence Usergroup



PREP SCHOOL
Avoid Silkscreen & silly escapes

International Cadence Usergroup



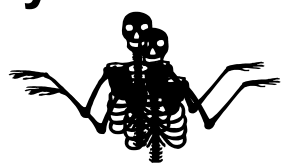
PREP SCHOOL POWER N GND

- **Time was when we only had 2 or 3 voltages and a couple of GNDS with wide distribution on the design.**
- **Now we are seeing large numbers with strange names**
- **Must deal with it up front**
  - **at least to define a complete list of nets that cannot just connect with the min. trace width.**
  - **All of these need to be identified and Specctra fixed or managed with trace width rules to stop Specctra completing hook ups with inappropriate min. trace.**
  - **If regions are used Specctra will obey the region rules!**

PREP SCHOOL POWER N GND

International Cadence Usergroup

- **Must deal with it up front (cont.)**
  - **Identify and plan cases of no moat crossing and nets that must stay in the shadow of an adjacent layer poly shape.**
    - **Really need the class/net keepin keepout feature**
  - **Identify and partition buried negative power layers and the shapes of positive planes on signal layers.**
    - **Watch out for Specctra duplicating these positives if a wire/route/ses file is written then read in.**
    - **Workaround = write -> unprotect delete poly then read.**



What do I know about version 15.0 ?

International Cadence Usergroup

- **Ran parallel testing in 15.0 of work done in 10.1 & 10.2**
  - **Lots of "I don't know yet".**
  - **A bit of not so good news**

  - **Some good news**

What about version 15.0 ?

- **Ran parallel testing in 15.0 of work done in 10.1 & 10.2**
  - **Lots of "I don't know yet".**
  - **Still have not looked at:**
    - **New net sets layer sets rule routing effectiveness**
    - **Pairs max length outside gap rule**
    - **Pairs region rules with max length outside gap rule**
    - **New attach vias and traces to poly wire and trace/via invasion of poly wires to reach a via.**

What about version 15.0 ?

International Cadence Usergroup

- Ran parallel testing in 15.0 of work done in 10.1 & 10.2
- A bit of NOT so good news:
  - Specctra auto route may crash and will converge quite differently if the status report is called while it is running.
    - Workaround never click for status report while running. Read the .sts file (note: you may have to make a copy of it to be able to read -- a windows thing).
    - That's the way we had to do it all the time in version 2!

What about version 15.0 ?

International Cadence Usergroup

- Ran parallel testing in 15.0 of work done in 10.1 & 10.2
- A bit of NOT so good news (cont.):
  - Specctra auto route CRASHED loading a dsn generated by 15.0 Allegro as migrated from 14.1. Specctra 10.2 does not crash reading in the dsn whether as generated by 14.1 or 15.0
    - Workaround stay in 14.2 and 10.2 if problem encountered. On migrations check that the new dsn and migrated rules will load before committing the design to the version upgrade.

What about version 15.0 ?

International Cadence Usergroup

- Ran parallel testing in 15.0 of work done in 10.1 & 10.2
- A bit of not so good news (cont.):
  - Problems with order violations particularly with virtual pin trees are still quite prevalent. Reporting and correction has still to be detailed manually in much the same way as I discussed at last years conference. (new test cases in)
  - Diff pairs and virtual pins were targets for this version. My preliminary results are on their combination disappointing. (Diff pair trees)

What about version 15.0 ?

International Cadence Usergroup

- **Ran parallel testing in 15.0 of work done in 10.1 & 10.2**
- **Some very good news**
  - **Notwithstanding the disappointments preceding They have held the line on performance so the new faster machines we buy will really speed us up. Overall the ROUTING QUALITY IS BETTER.**
    - **Than was not the case when we left fast stepping sexy six behind.**
    - **The checks I ran showed a little up here and a little down there, both on run times, and completion %**

What about version 15.0 ?

International Cadence Usergroup

- Ran parallel testing in 15.0 of work done in 10.1 & 10.2
- Some good news (cont.)
  - The “connector refuses to connect” is solved in 15 as detailed earlier.
  - No license problems to date.
  - The quality is very much better than it was the year of the 101 V9 damnations. It took many hours of testing to find any crashes or hangs
    - 17 V15 problems reported to date including 2 crashes and a hang. (compares to 41 V10)

What about version 15.0 ?

International Cadence Usergroup

- **My FAVORITE is what has been done to miter**
  - **I get the request "keep the routing as short as possible" all the time. (CIAR)**
  - **Based advice from Jud Lane many years ago we evolved a progressive miter, but still required HOURS of CLEANUP**
  - **Adding that progressive to the new miter with passes v15 Specctra gives something that is MUCH MUCH closer to "keep the routing as short as possible"**
- **Lets take a look at progress.**

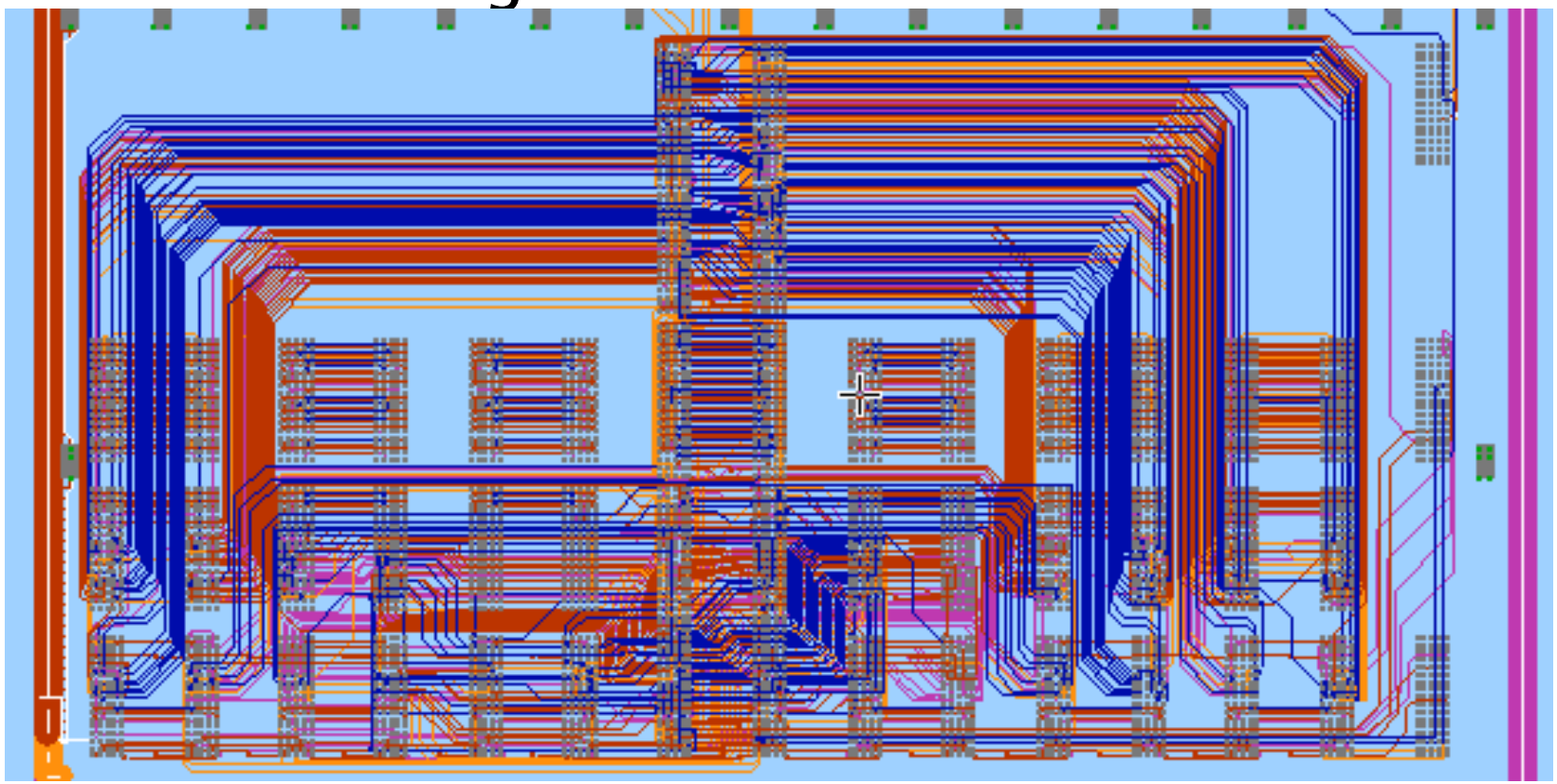
FIRST -- What does progressive MITER MEAN?

- **Default means “miter” or used “miter 100” v15**
- **Progressive means: (over 50 commands)**
  - `miter 100 (bend 3000 2000)`
  - `miter 100 (bend 2000 1000)`
  - `----------`
  - `miter 100 (bend 40 40)`
  - `miter 100 (bend 39 39)`
  - `----------`
  - `miter 100 (bend 6 6)`
  - `miter 100 (bend 5 5)`

DEFAULT MITER IN version 10.1

International Cadence Usergroup

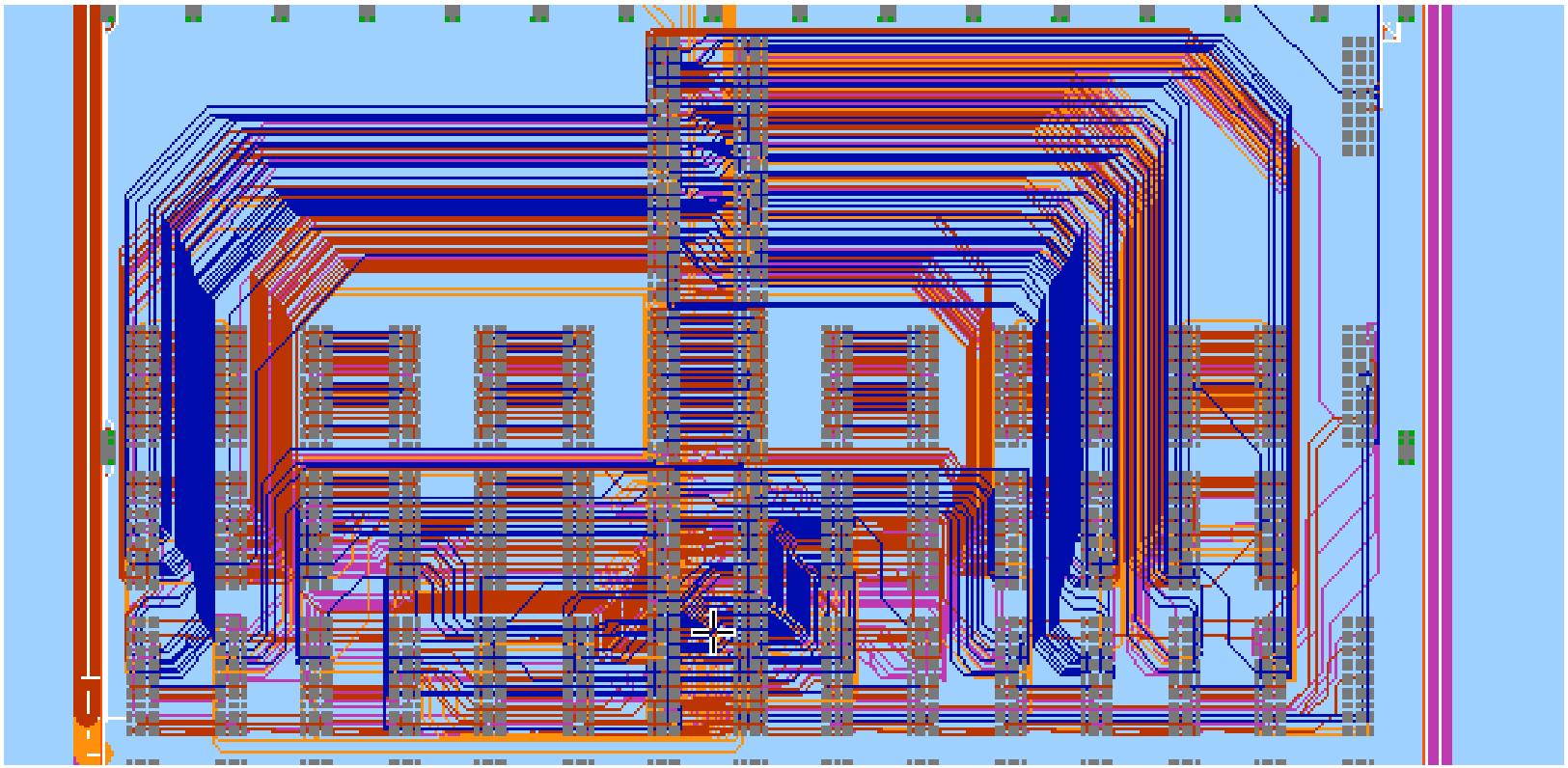
- Routed length=288503.843 Ratio 1.0432



progressive MITER IN version 10.1

International Cadence Usergroup

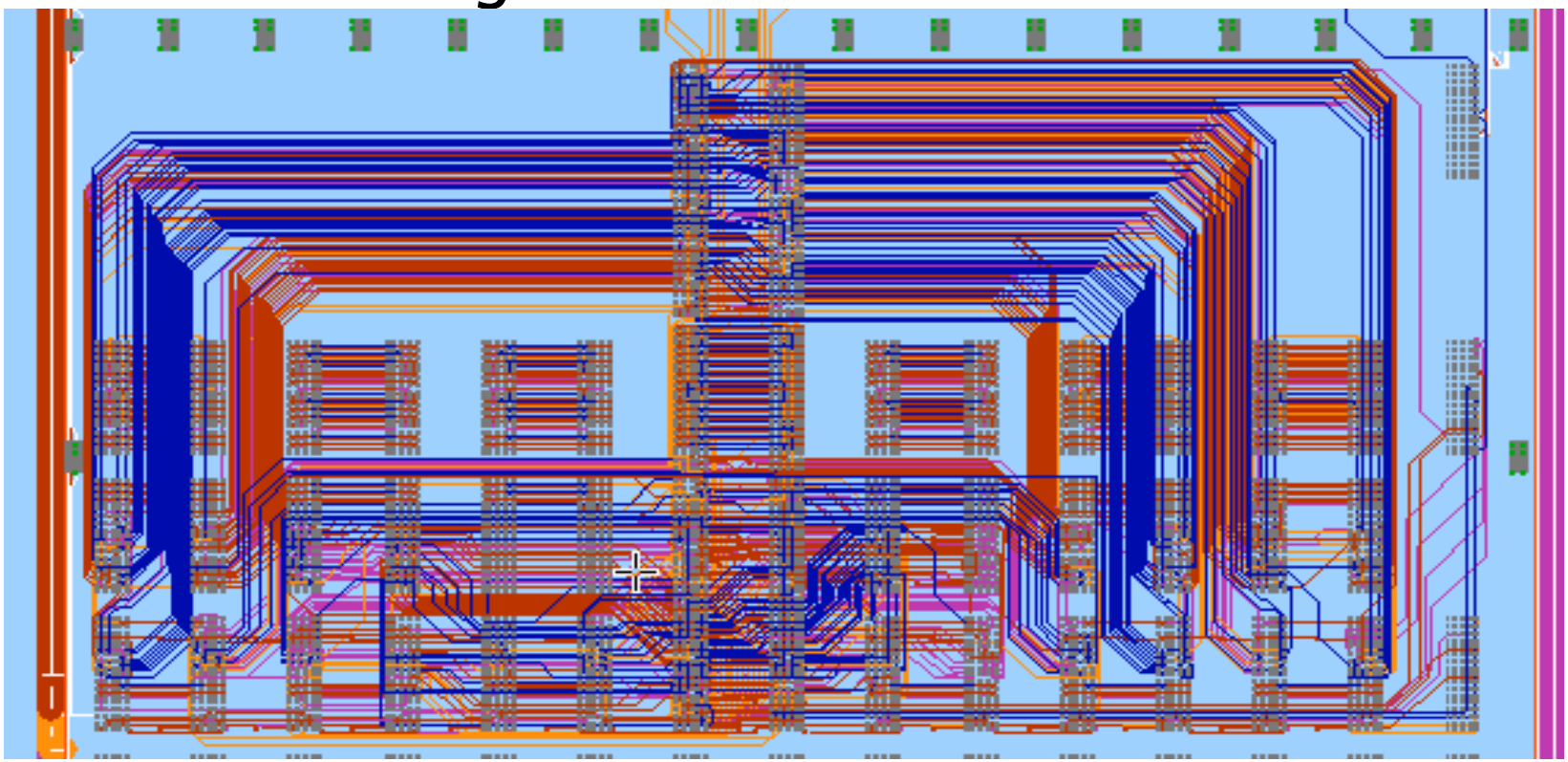
- Routed length=284712.372Ratio 1.0295



Default MITER 100 IN version 15.0

International Cadence Usergroup

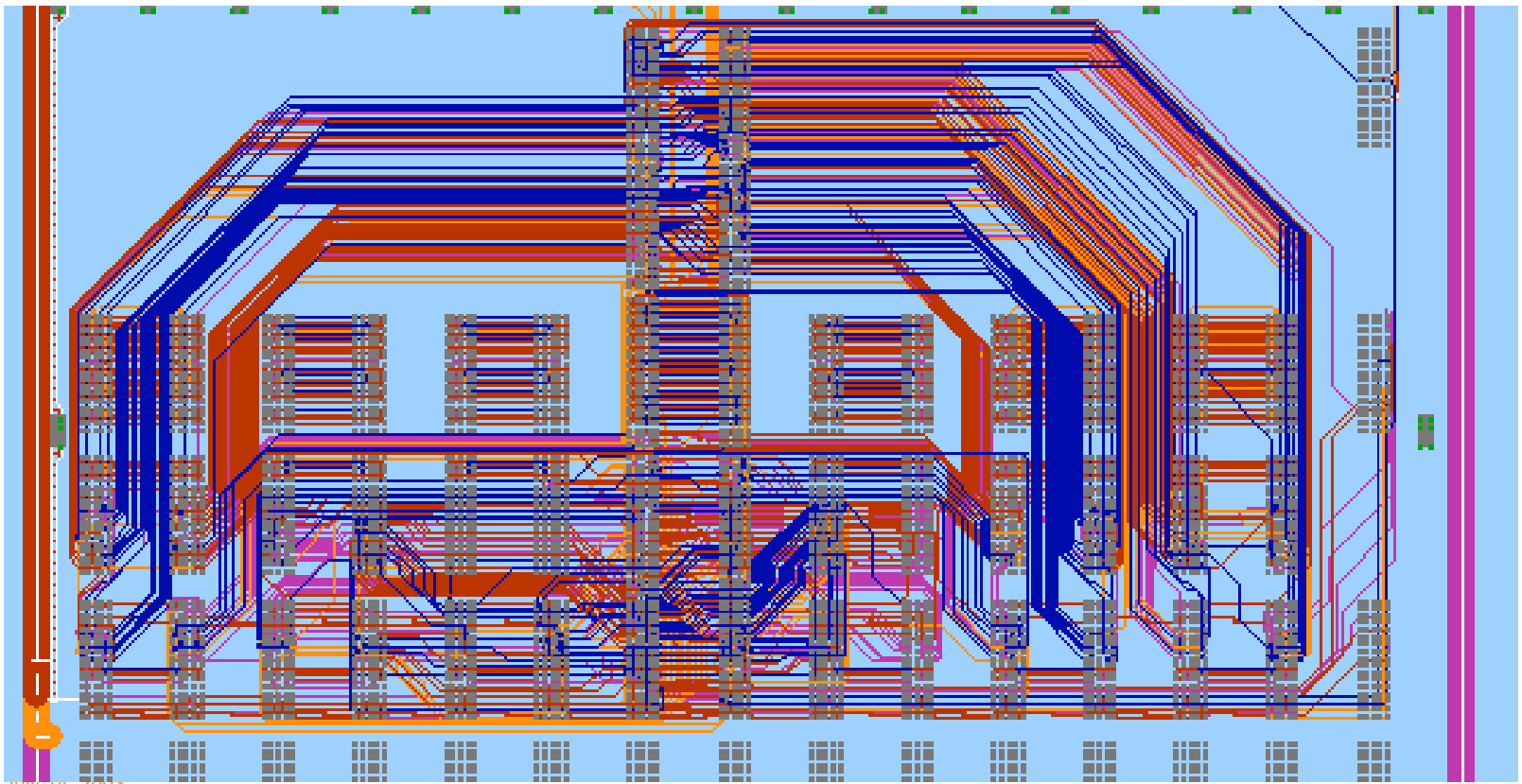
- Routed length=286644.736 Ratio 1.0365



progressive MITER IN version 15.0

International Cadence Usergroup

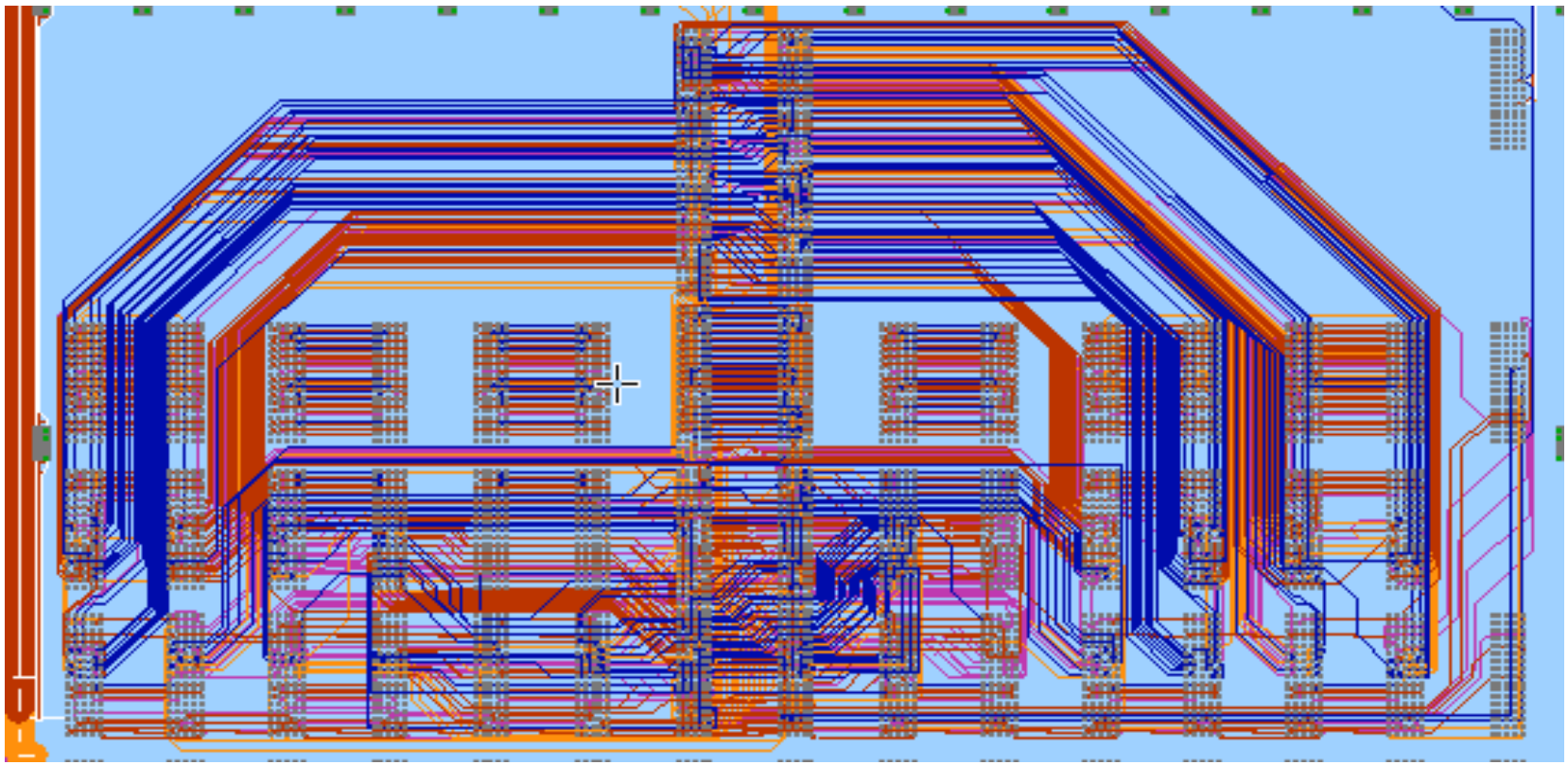
- Routed length=274450.505 Ratio 0.9924



progressive MITER IN version 15.0 + 10 min. cleanup

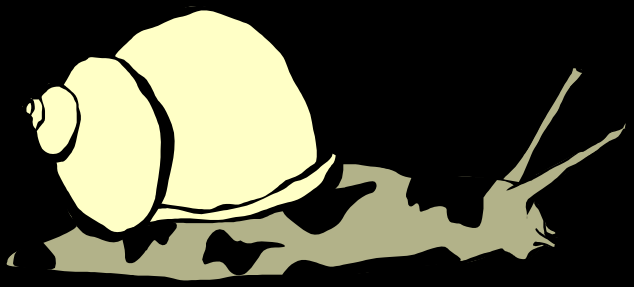
International Cadence Usergroup

- Routed length=273585.565 Ratio 0.9892

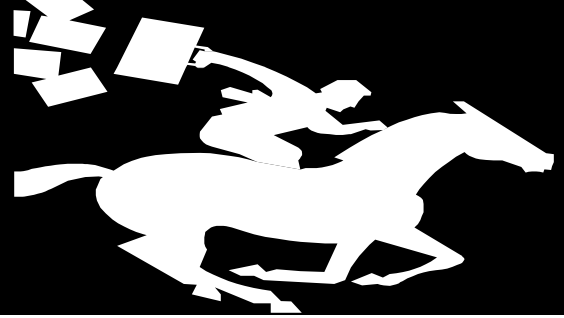


MITER PROGRESS 2001 > 2003

	DEFAULT		PROGESSIVE	
	LENGTH (m)	RATIO	LENGTH	RATIO
V9.2	290.6	1.0508	287.7	1.0406
V10.1	288.5	1.0432	284.7	1.0295
V15.0	286.6	1.0365	274.4	0.9924
Before miter			298.9	1.0806
With miter + cleanup			273.5	0.9892



Bye



If no more questions then

ME