General Overview

- **Brief update on PROGRESS fixes & improvements by CADENCE in release 10.2 and release 15.0**
- **TEST POINTS WHY and HOW**
- **Auto routing silkscreen?**
- **When Specctra goes AWOL on ORDERS**
  - **Ways to lure it back,**
  - **Avoiding being run over by a BUS**

Update On Progress In Release 10

Quality getting better

- **We reported 110 problems on release. 9 with, many fixed in release 9.03 and the MAJORITY of which are FIXED IN RELEASE 10**
- **This COMPARES with 41 found in release 10 with testing starting in beta on both releases with our level of testing effort approximately. Equal per release.**
- **Of the 41 -- 14 fixed, 5 promised in release 15.1, 4 have workarounds. Some were just reported recently so this is clearly progress. CORE DUMPS GONE AWAY DOWN.**
- **Virtual pins, pairs, bundles, 45 degrees, regions, and performance are still fragile.**

Update On Progress In Release 10

PROBLEM LIST

- **Prob1:Mon 11/20/00 crashes showing a release 9.03 problem still in release 10: select all nets, report, specify, selected, you crash.**
  Rated: Important
  Status: FIXED

- **Prob2:Mon 11/20/00 when the system crashes in release 10 on the PC it does not release the license.**
  Rated: Critical
  Status: FIXED

- **Prob3 Fri 11/24/00 suddenly jumping up by 2000 clearance violations which it struggled unsuccessfully for hours.**
  Rated: Important
  Status: FIXED

- **Prob4 wed 11/29/00 SPECCTRA shape based automation software does not support license usage any more. Please use "sh lmstat -a" command instead.**
  Status: ? Licensing to be overhauled in 15.0

- **Prob5 Thurs 1/18/01 NET REPORT for the net incorrectly shows the min length from the class as the min rule in effect. It shows it as a class rule and fails to show the min net rule number although the net rule is controlling the operation.**
  Rated: Important
  Status: OPEN - Report rules all is correct though

Update On Progress In Release 10

PROBLEM LIST

- **Prob6 Fri 1/26/01 move creating crosses with checking on when crosstalk rules are in effect.**
  Rated: Important
  Status: OPEN

- **Prob7 system variables flip flop integer to string breaks do file logic in if & while constructs.**
  Status: FIXED

- **Prob8 Thurs 4/19/01 bad routing caused by a false keepout under the FPGA.**
  Rated: Important
  Status: FIXED

- **Prob9 Mon 4/23/01 unconnect left by release 10 not happening in release 9 and earlier releases.**
  Status: OPEN

- **Prob10 a) Thurs 5/24/01 virtual pin design crashes in both release 9.03 rel10.02 status (workaround: set bay_virtual_pin on)**
  Rated: Critical
  Status: FIXED (default is on in release. 10.2)

Update On Progress In Release 10

PROBLEM LIST

- **Prob10 b) Thurs 5/24/01 NT/PC puts the diagnostics in temp directory and defaults others?? If not $\. all outputs should default to the folder containing the .Dsn (some now do)**
  Status: ? seems better in late releases.

- **Prob10 c) Thurs 5/24/01 NT/PC crashes you cannot scroll back in the output window.**
  Status: Workaround: use output option at startup

- **Prob10 d) Thurs 5/24/01 set command set bay_virtual_pin is not documented and the default is wrong (quite a few not documented).**
  Rated: Important
  Status: OPEN

- **Prob11 Fri 6/8/01 The many wiggles of 0.5 mil in the pairs destroy the gap integrity. Not in release 9 but trombones are still added to one of the pair wires to match them. "Turn pair averaging on to avoid this behavior."**
  Rated: Critical
  Status: FIXED

- **Prob12 Fri 6/8/01 clean increases the number of length violations also true in release 9.**
  Status: UNKNOWN

Update On Progress In Release 10

PROBLEM LIST

- **Prob13 Fri 6/8/01 miter increasing length violations to the same level as release 9 giving back all the gains made by the route command in length rule compliance.**
  Rated: Important
  Status: FIXED

- **Prob14 Fri 6/8/01 miter creates many gap violations ie the gap in the pair mitered corner far greater than the specified gap.**
  Rated: Important
  Status: FIXED 98%

- **Prob15 Fri 6/8/01 The move in pushes the corner of a pair trombone and the inner trombone collapses all the way back to the straight.**
  Rated: Important
  Status: OPEN 15.0?

- **Prob16 Fri 6/8/01 pair gap is greater than rule, router unaware, not inform the user that it has a problem. Should highlight.**
  Status: OPEN THE PAIR APPROACH IN RELEASE 15.0 MAY ADDRESS THIS ISSUE

- **Prob17 6/8/01 The rule (length_amplitude 0) not working right in release 10.**
  Rated: Important
  Status: Seems to be FIXED. Only using trombone pattern now.

Update On Progress In Release 10

PROBLEM LIST

- **Prob18 Tue 6/26/01 The unconnect count relative to release 9.**
  Rated: Important
  Status: UNKNOWN

- **prob21 9/20/01 release 10 core dumps on hp out of swap release 9 and earlier gives out of swap message and no core dump.**
  Rated: Important
  Status: SUBMITTED

- **Prob22 9/25/01 Rel 10.1.1 100% slower than release 9.03 and 340% slower than release 6 Specctra on HP release 11.**
  Rated: Critical
  Status: FIXED IN REL 10.2

- **Prob23 12/21/01 The bus command in this instance is creating parallel crosstalk rule violations.**
  While this is not appropriate it is rated as a minor problem because the router does realize that a conflict has been created.
  Rated: Minor
  Status: OPEN

Update On Progress In Release 10

PROBLEM LIST

- **Prob24 11/13/01 Release 10.1.1 HP rel10 current net display intermittent The current net shows with measure, edit, and move some times and not sometimes. resizing the window seems to restart it to work for a while.**
  Rated: Important
  Status: OPEN

- **Prob25 12/21/01 Bus is putting traces in with the wrong width – net rule –no width check.**
  Rated: Critical
  Status: OPEN (W/A stopped using the bus command on high speed designs)

- **Prob26 12/21/01 Test point spacing rule migrating to internal layers on vias containing a test point causing the route to fail on the internal layers. In this case have a wire_via clearance 4.5 internally and 5.0 externally. The corollary is that if we routed the board then tried to use specctra to apply test points it would probably fail because it would then incorrectly consider that adding the test point to a quite legitimate via would violate clearance and so not.**
  Rated: Very important
  Status: UNKNOWN

- **Prob27-1 12/21/01 Measure is pointing to the wrong rule and defining it incorrectly.**
  Rated: Important
  Status: UNKNOWN

Update On Progress In Release 10

PROBLEM LIST

- **Prob27-2 4/17/02. FALSE ORDER VIOLATIONS REPORTED**

Specctra falsely reports 145 order violations requiring manual detailed checking of nets that are are routed out of order or with stub length faults. In the main router run170 were reported at the end of which 25 were real to be fixed in cleanup.The problem is that 145 had to be individually inspected and referenced to the rule to determine that they were not violating.
Rated: Very critical
Status: OPEN

- **Prob28 12/21/01 The format of the Wire-Via Clearance reported by measure should be consistent with the format of Wire_Via Clearance as in the report rules. (facilitate copy and paste)**

Rated: Minor
Status: OPEN

- **Prob29 4/17/02 This case deals with an example of power in this design that is blatant. During the routing of the regular nets we encountered cases of regular nets doing the same thing. The router fails to make connections on nets with many pins until repair net is run-- then it works better some times require a few iterations of repair net then route.**

Rated: Very important
Status: UNKNOWN

Update On Progress In Release 10

PROBLEM LIST

- **Prob30 4/17/02 Pop up window for measure is inadequate for its intent Tests in PROB28 involve using measure in a trouble shooting situation. There are no scroll bars or resizing capability on the pop up making it just some thing to turn off and use the output message window most of the time. This feature would be more useful if resizing and scroll bar were included. It is a good idea but the implementation falls short. Search capability on it would give it a useful advantage over the output window for this function. Note: This is ok on Unix (needs search) but the NT version I am using is not ok.**
  Rated: Minor
  Status: UNKNOWN

- **Prob31 4/17/02 Measure lost its ability to examine pins. Measure was always able to identify virtually anything on the board including pins up to and including release 9. With release 10, it lost its taste for pins making it inferior to the previous releases in this respect.**
  Rated: Important
  Status: FIXED in release 10.2

- **Prob32 4/17/02 The selected feature is missed on the unconnect report. Reference PROB29 w/a copy the directory and change the do file to fix all other nets and not just route the 2 power classes to see after 5 passes and pause and stop -- see how helpful the ability to report unconnects selected would be.**
  Rated: Important
  Status: UNKNOWN

Update On Progress In Release 10

PROBLEM LIST

- **Prob33 4/17/02 This identifies the fact that the poly duplication detailed in PROB27-2 for wire files also occurs with both route and session files.**
  Rated: Very critical
  Status: UNKNOWN

- **Prob33b 5/14/02 The commands no longer come out on the start up window nor in the did file nor in the console log file (-O option on command line startup).**
  Rated: Very important.
  Status: FIX PROMISED in 15.1 and workaround suggested: Once the session is started the command vdo on either from the command window or in the do file will cause Specctra to revert to the behavior of recording things in the command window etc. as required.

- **Prob34 6/26/2 specctra fails to route dsn generated by Allegro 14.2 but routes dsn generated by Allegro 14.1. The case found involved the connector being used to attach daughter boards to mother boards and is known as an NEXLEV connector. It may occur with any other devices with a dice 5 pattern that is not on true 45 or 90 degree pin and therefore via configuration.**
  Rated: Very important
  Status: ACCEPTED. In the meantime we are using Allegro release 14.1 to generate the dsn.

Update On Progress In Release 10

PROBLEM LIST

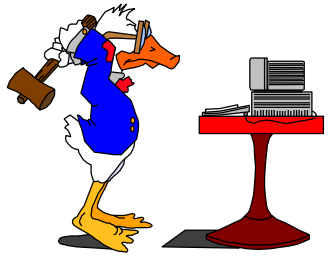
- **Problem NULL Part way through a series of fanout commands the router starts deleting an orphan shape of a keep out at each pass and thereafter the router fails to use any vias and therefore fails to route the board.**
  Status: THIS PROBLEM EXISTS IN V10.1 BUT IS FIXED IN V10.2

- **Problem ? Diff pairs max length on each member different will take the first one defined of the pair if length rule is after pair definition. W/A define length rule before pair definition. Reorder the rule do file for these.**
  Rated: Critical.
  Status: TO BE REPORTED

- **Problem ? Class length definition of ratio applies the ratio to the longest net in the class and sets that as the max length for each net in class.**
  Rated: Very important. Work around: select class and set rule selected.
  Status: TO BE REPORTED

- **Problem ? Order violations not reporting violations of the order rules.**
  Rated: Critical.
  Status: TO BE REPORTED

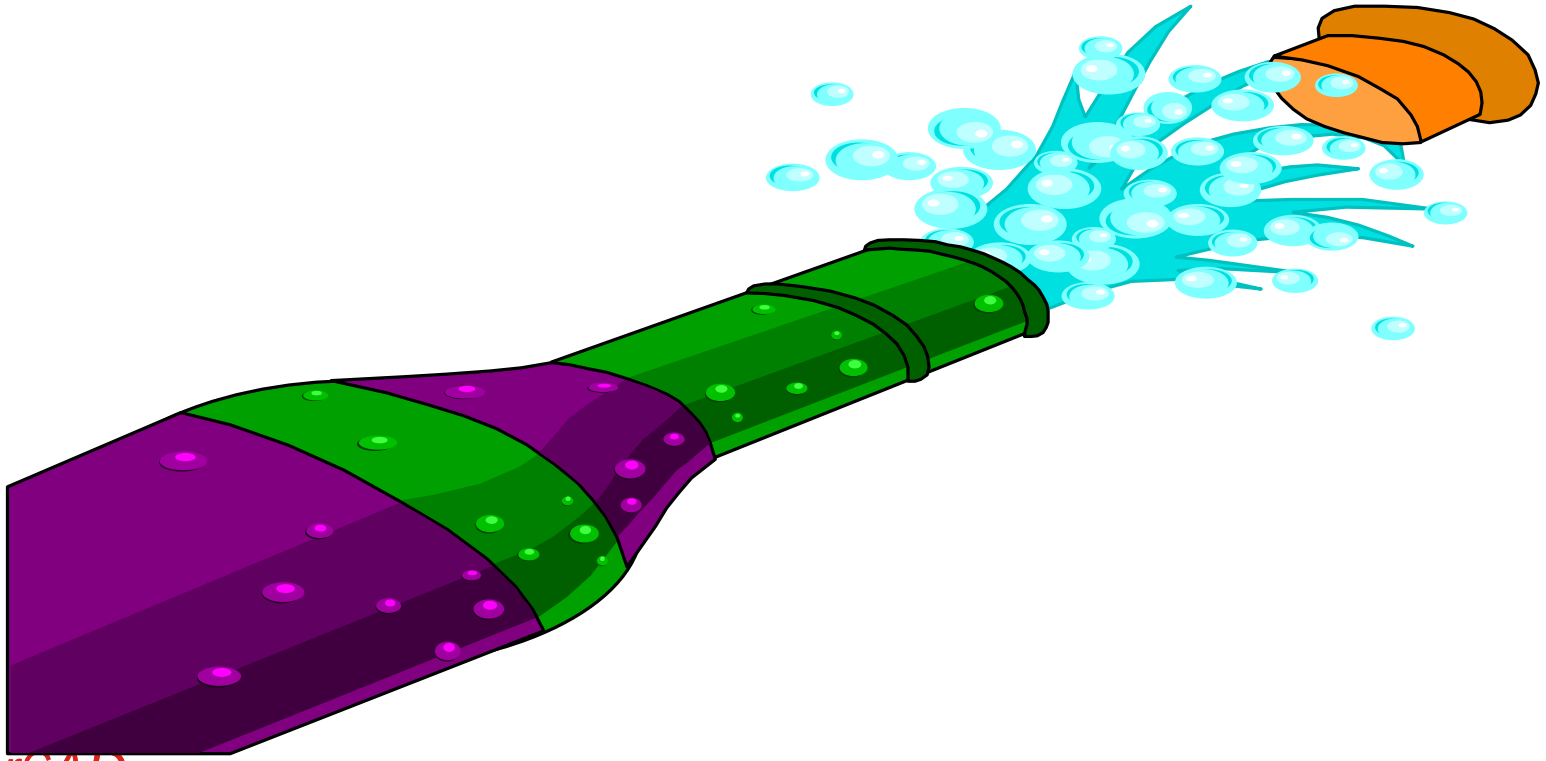
DEADLY PROBLEM 6,7,8,9,EARLY 10



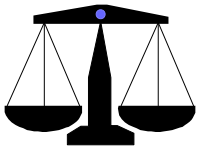
- **IF AND WHILE CONSTRUCTS USING CONFLICT_WIRE OR UNCONNECT_WIRE.**
- **Specctra contains something called system variables which can be used in do files that run all weekend to do different strategies depending on whether things are stalled or progressing. Examples are in the user manual and in papers on expert level use of Specctra.**
- **Most do files we use contain some if's or whiles.**
- **If a do file using == or != or >= referring TO these is running and you use the monopoly card to see the status, sometime later when the if or while executes (like after you went home) it would either crash or continue with a wrong interpretation of the logic.**

DEADLY PROBLEM 6,7,8,9,EARLY 10.2

- **FIXED IN LATER REL. 10**



Test points WHY?



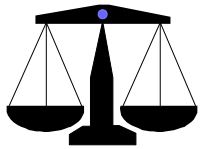
NOT TO PROVE THAT THE DESIGN WORKS!.

- That takes place long before volume manufacture.
- Designs with high speed circuits will not work with a bed of nails in place. (signal integrity is shot)
- Proving that a particular board works happens in system test.

So WHY are the Production folks so adamant?

- In design we have to get it right ONCE for any product. They must get it right up to MILLIONS of times and MAKE MONEY IN THE PROCESS!
- From time to time component suppliers, machines, and people get it wrong!
- Then they must identify the source of the failure.

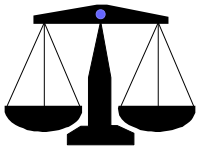
Test points WHY?



WHY the Production folks are so adamant

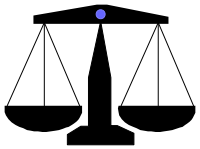
- Then they must identify the failure and the source of the failure fast.
  - Defective component?
  - Defective process?
  - Information data /instruction wrong or misunderstood?
  - Components swapped or rotated incorrectly?
  - Isolated instance or rampant with 1000's of the same defect?
  - Intermittent hardware in one of their many processes.
  - Intermittent software ("has a bug" happens in their world too).
  - Contamination of process materials, in supplier material, or in the production or storage environment.
  - I will not bore you listing all the many possible causes.

Test points WHY?



- **WHY the Production folks are so adamant**
  - **Then they must correct the source and minimize their losses.**
  - **If there are many defective assembled boards, their repair is not just a question of cost, but a question of time, to meet delivery commitments and keep their customers from going elsewhere.**
  - **In their world customers can switch to another provider even more easily than in ours.**
- **Their testing capability is their first line of defense**
  - **It must be as COMPLETE and ROBUST as possible.**

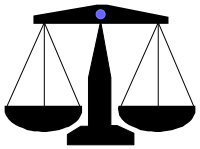
Test points HOW?



Go FOR 100% RIGHT AT THE GET GO

- Take all the FREE ONES FIRST
  - All through hole wide pitch pins are free ones -- be very sure you have them all. (connectors!!)
  - If Jtag (or other new techniques) is used make sure the list of nets covered is identified and avoid test pointing them.
- Unused pins are the most difficult, resolve them next.
  - ONE place to go, but can usually tolerate some antenna.
  - A 48v short to an unused gate pin on a BGA that operates at 1.5 can toast the whole thing or worse make it intermittent.
  - On the other hand a pin connected to nothing inside really does not need a test point. Identify those as such.
  - Officially Specctra does not handle these but fanout with appropriate rules and keepouts can be used to get them in.

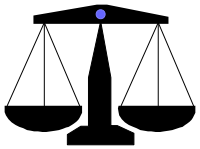
Test points HOW?



Go FOR 100% RIGHT AT THE GET GO

- Unused pins are the most difficult, resolve them next.
  - Do a dummy fanout unused to get the net defined then set up the rules to the net +unused+ orphan_net. Do the real fanout of unused. The net unused orphan rules keep the other test points spaced away. Remember you need keepouts under devices on the bottom of the board during this fanout process.
  - If things are very congested in the BGA and unused pins are causing the test pointing to fail:
    - Consult with the circuit designer and test engineering folks. In some it may be possible to connect 4 adjacent or 2 or even 1 to a single gnd via with everybody happy.
  - Minor tweaks of (component/pre route fanouts) placement particularly on the bottom are easy at this stage -- not so if test pointing is done either at the end or in process (if pre fanouts).

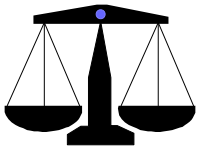
Test points HOW?



Go FOR 100% RIGHT AT THE GET GO

- 2 pin nets on high speed or limit via 0 classes are the next most difficult, and important to avoid antennas so resolve them next.
  - For the first pass use a rule or keep out to prevent use of BGA and restrict to vias if pre fanouts are involved.
  - If pre fanouts are not involved use rules to limit the test point reach out.
  - If component or via placement changes needed do them now.
  - Now let it have access to the BGA vias for these 2 pin guys.
- Next test point all BGA nets restricting the process to not use BGA vias on the first pass.
  - If component placement or via tweaks will get some in not on the BGA -- do it now.

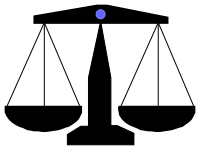
Test points HOW?



Go FOR 100% RIGHT AT THE GET GO

- **NOW FOR THE BIG ONE– the nets appearing only on the BGAs :**
- **IF you have a mix of 50 mil and 1 mm and 0.8 mm BGAs Then: 2 pin nets – high speed - limit via 0 first next staging through nets with increased possibilities.**
  - **Be sure to save what you have and try to push though on 70 mil pitch.**
  - **If you get there it is a good day and you will have happy folks all around.**
  - **If not then drop to 50 mil for what is left restricting it to the 50 mil pitch BGA on the first pass and opening up the mm guys on the second pass.**
  - **If that fails back up (backing out all the 70's on BGAs) and try for the BGAs at 50 with the same first and 2nd pass strategy.**

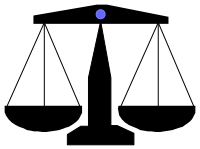
Test points HOW?



Go FOR 100% RIGHT AT THE GET GO

- **Benefits of this strategy:**
  - **If you really need something like Jtag or other approach you find out when there might just be time to get it done.**
  - **If there are some pre routes on top of the board that test points were forgotten on it is less painful early. (Basic rule on pre routes – if you must have them then do the whole job including testpoints). This includes nets pre routed entirely on the bottom therefore having no vias. Space?**
  - **By doing the most difficult and critical nets first there is a good chance that what is left might just tolerate short antennas.**
  - **There is often a last minute rush to release the design and doing testpoints in that period will not get the coverage or limit the number of 50 mil pitch pins on the bed of nails like do it at the beginning can.**

Test points HOW?



Go FOR 100% RIGHT AT THE GET GO

- **Benefits of this strategy:**
  - **You will get the highest percent coverage possible and avoid using the more fragile small diameter test probes than necessary.**
  - **Most of the time 100% coverage really is possible!**
  - **You survive when less than 100% is simply not acceptable.**
- **Those manufacturing folks will welcome your design and might just make money building it.**

AUTO ROUTING SILKSCREEN?

MORE ACCURATELY AROUND SILKSCREEN

- OVER THE PAST 20 YEARS MANY PEOPLE HAVE TRIED TO MAKE SILKSCREEN GO AWAY.
- It's like taxes (we have to live with it).
- I remember one Design Engineer who hated it.
  - Got himself promoted to the top power position in a large manufacturing facility.
  - Authorized the removal of silkscreen form his product line.
  - Result: He lost his job and the product line had the silkscreen put back in as before.
- It's not going away! So lets find the least painful way to live with it.
- In production it is a low cost trouble shooting tool.

AUTO ROUTING SILKSCREEN?

MORE ACCURATELY AROUND SILKSCREEN

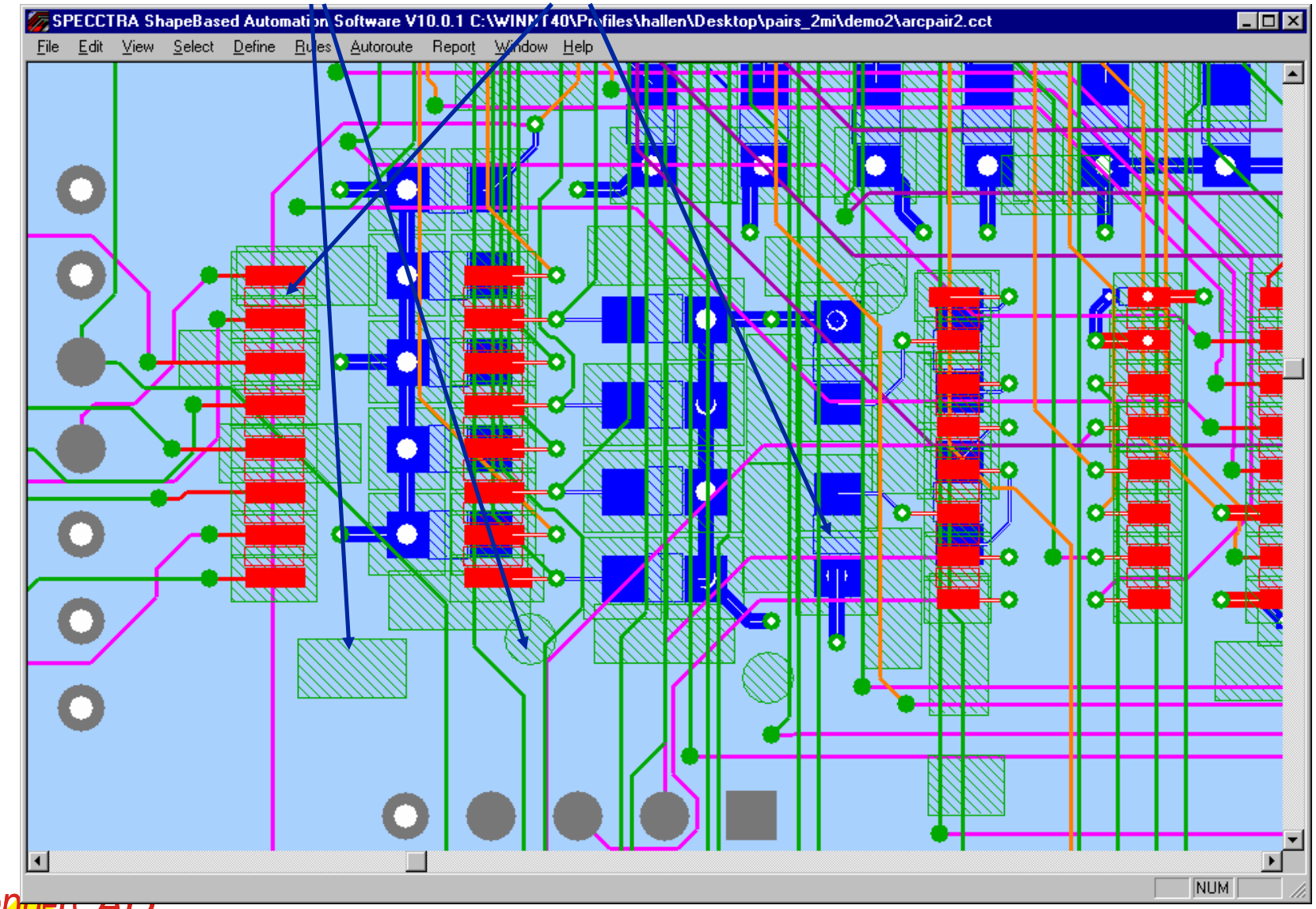
- **DO IT EARLY right along with placement.**
  - **Minor placement adjustments can make it a lot easier.**
  - **Put it in smart locations to minimize blocking via sites.**
- **Apply via keepouts with skill software that are 10 mil larger before going to the auto router.**
- **If there are any (usually less than 1%) that are blocking vias in congested areas either remove the keep out in Specctra and continue, or move the silkscreen to a smarter location in the host tool.**
- **Once again you avoid fighting with silkscreen at the end, getting a inferior result and the stress at the end.**

AUTO ROUTING SILKSCREEN?

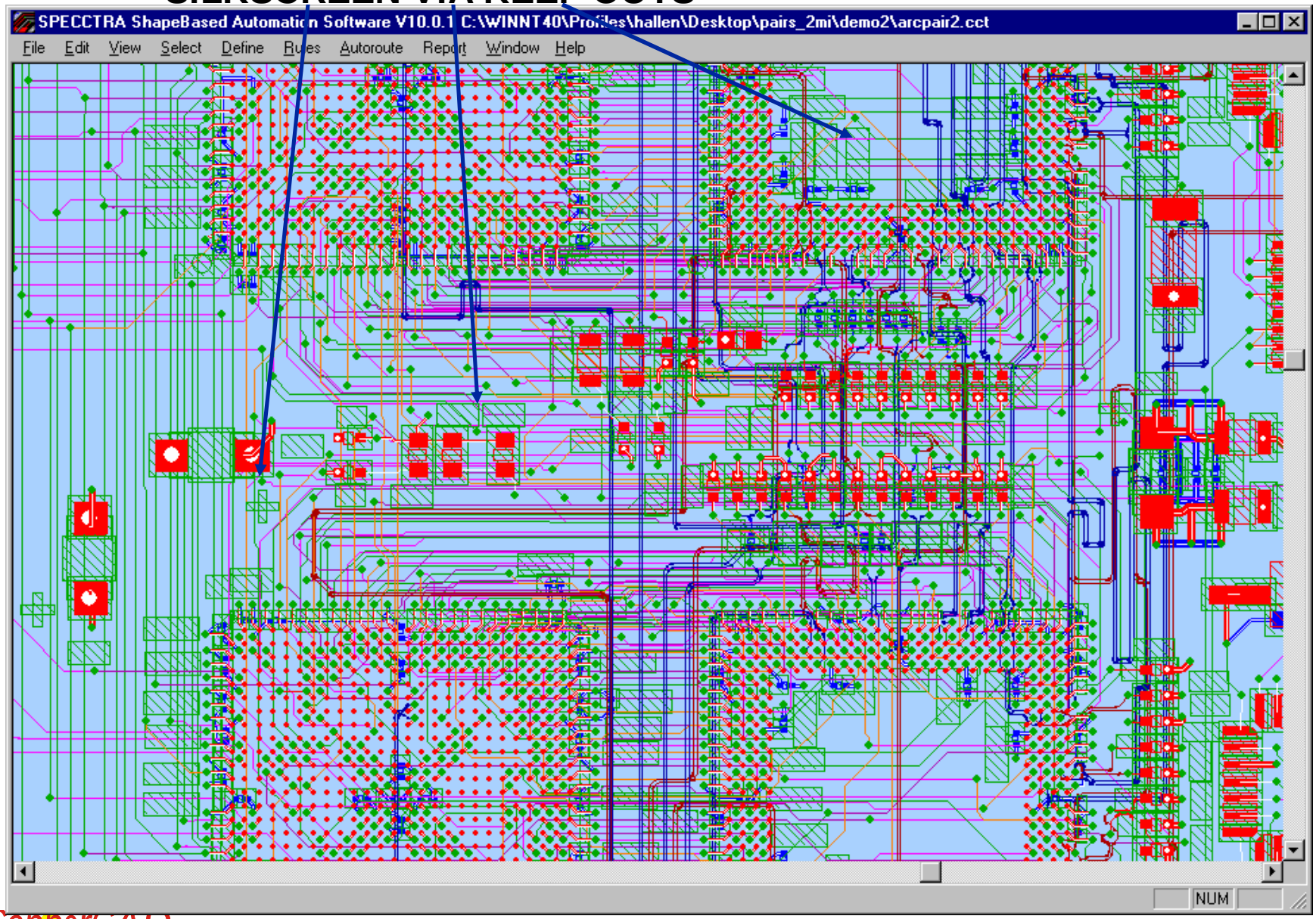
MORE ACCURATELY AROUND SILKSCREEN

- I have compared auto route runs with and without the silk screen associated keepouts.
  - The total routed length for the board shows little difference.
  - A couple of inches on a 5000 inch total.
  - In some cases it is over all shorter with the keepouts in!
- As always there are exceptions but:
  - These are in some very congested area's on the board not the whole board and many boards have no exceptions.
  - The small discretes directly under BGAs are such exceptions in some cases. (common sense applies)

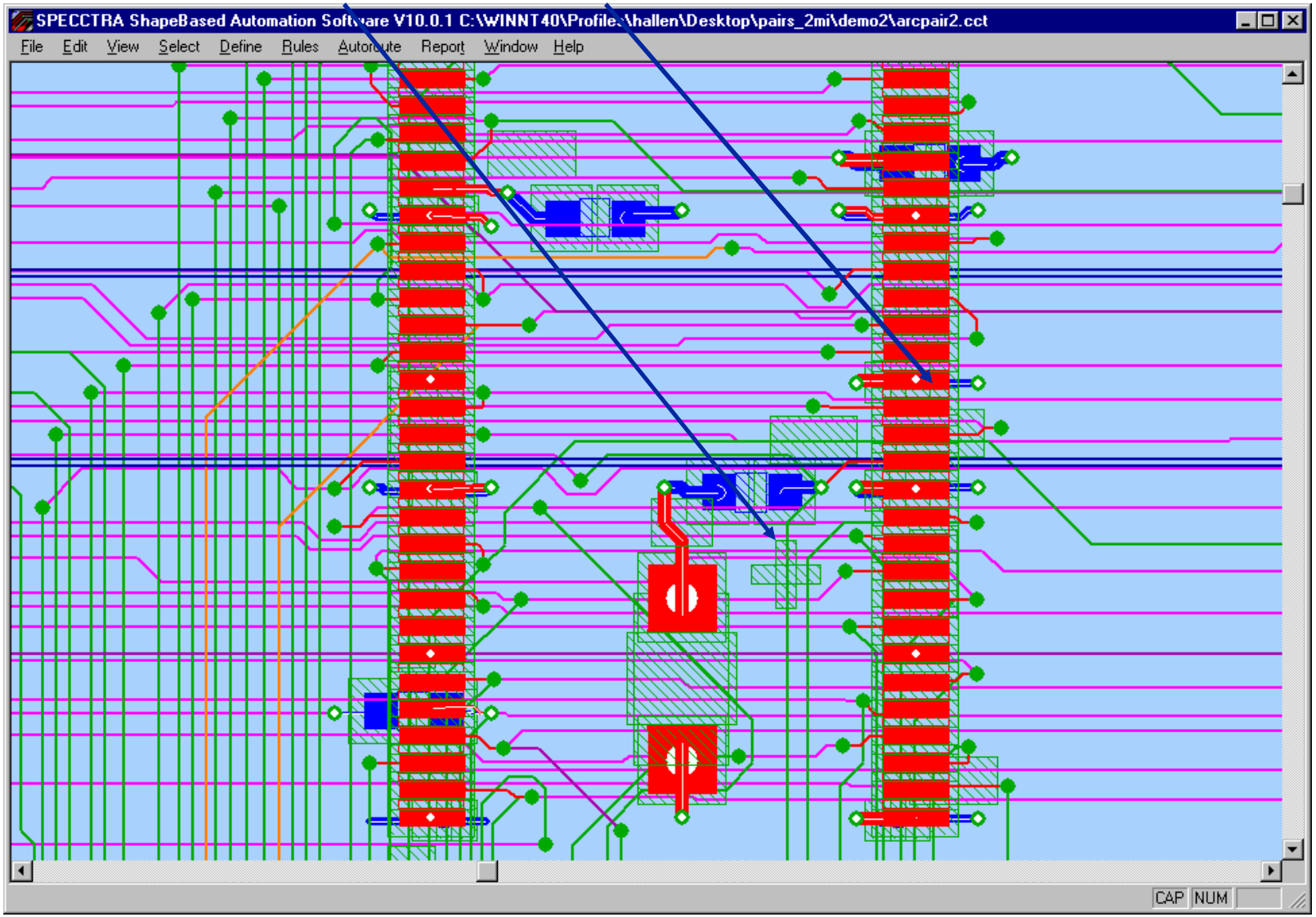
SOFTWARE GENERATED KEEPOUTS SOLVE SILKSCREEN & FANOUT PROBLEMS



SILKSCREEN VIA KEEP OUTS



SOFTWARE GENERATED KEEPOUTS SOLVE SILKSCREEN & FANOUT PROBLEMS



When Specctra goes AWLO on ORDERS

WAS wounded badly BY this ONE VERY recently!

- Order violations report is reporting false violations.
- Order violations report is not reporting real violations.

- Now our customer gives us the schematic and the constraint definition to open the deal.
- We give back the .brd file etc. and Specctra reports that confirm constraints met to close the deal.
  - The length report (with its select feature) does a wonderful job in this. Used to negotiate concessions during the process.
  - The all rules report – wonderful (closing the loop)
  - Conflicts report – wonderful (only give it when saying none)
  - Network report (with its select feature) – wonderful

When Specctra goes AWLO on ORDERS

- **Cannot give the order violations report and the notations on the length report re order violations are embarrassing. Both wrong and inconsistent.**
  - **Ditto for the notations on the bottom of the status report re order and stub.**
- **Have a reasonable workaround to visually check all order constraints and report (will show later)**
  - **Can check and record about 4 per minute so even 500 to 1000 nets are doable this way.**
- **Currently testing on current designs with release 10.1, 10.2 and later.**

When Specctra goes AWLO on ORDERS

- **I am currently part way through determining what the causes are! (some may be me but which ones?)**
  - **Have submitted test cases on this going back as far as release 7 but in fairness it is quite confusing with its many variations.**
    - **Daisy chains vs. fromto's or combined or with virtual pins**
    - **Pairs vs. single ended**
    - **As auto routed vs. from wire file vs. pre routes vs. interactive**
    - **Rule priority in the hierarchy in Specctra and vs. host**
    - **Debris coming in from the host (Redundant segments)**
      - **Tiny dangling ends and redundancies hidden in pads seen as loops and order violations although well within stub.**
      - **Bad rule definitions & Redundant rule definitions**
      - **Mixed rule definitions etc.**

When Specctra goes AWLO on ORDERS

So far it SEEMS THAT Sometimes :

- Combining a daisy definition with a specific fromto ie. Partial order definition will fail. It seems to work some times but that is probably coincidence (the shortest ==).
- Defining a class order and using a net rule to over ride the order of the class for that net is questionable.
- If specctra gets it wrong it does not realize its wrong. It will put it back wrong in an open area (following a wire delete of wrong order that shows the guides right after the delete!).
- Tiny discontinuities in pre routes confuse the order check whether in complete net pre routes or in partial such as pre route fanouts with via sharing.

When Specctra goes AWLO on ORDERS

So far it SEEMS THAT Sometimes:

- Tends to get it wrong in congested areas particularly when first laying the route in. That would be normal and ok if it only realized the error and tried to correct it later on and reported it correctly throughout.
- Tends to get it wrong if net carries length constraints as well as order when these are difficult in unison. This is common if the length constraint requires miter to achieve.
- Tends to get it wrong if the required order is much longer that the min possible manhattan for the net.

When Specctra goes AWOL on ORDERS

Ways to lure Specctra back: setup

- Do not mix daisy definitions with fromto order definitions
- Do not change order rules on the fly. Use a reload and complete rule regeneration if an order rule needs to be changed. (Delete wires of nets to be changed before writing wire file)
- Keep the order rule definition simple and single level. Do not assume that the normal rule hierarchy is working.
- If any order in the net defined at the group or fromto level then define the order for the whole net at this level.

When Specctra goes AWOL on ORDERS

Ways to lure Specctra back: setup

- For daisy chain use the following unambiguous syntax, makes visual check simpler as well.
  - `rule class uxyz (tjunction off)`
  - `rule class uxyz (max_stub 200)`
  - `define (class uxyz (topology (comp_order Ux Uy Uz)))`
- For pairs define order at the net level prior to defining the pair as a pair.
- Check and replace/delay rule.do file related stuff.

Some of the above may not be necessary. For the moment cannot use rifle (cracked scope), so must use shot gun at close range.

When Specctra goes AWOL on ORDERS

Ways to lure Specctra back: (Nursing the run)

- Get specctra to commit itself to the order you want by:
  - Not telling Specctra about length constraints in the beginning of the routing.
  - Select classes nets etc. with order rules first and route for a while.
  - If there are some with layer use or via limits constraints do them first.
  - Then without protecting them add the rest to the mix.
  - When that is digested successfully add the length constraints to the ordered nets.
  - Then length constraints for the rest.

When Specctra goes AWOL on ORDERS

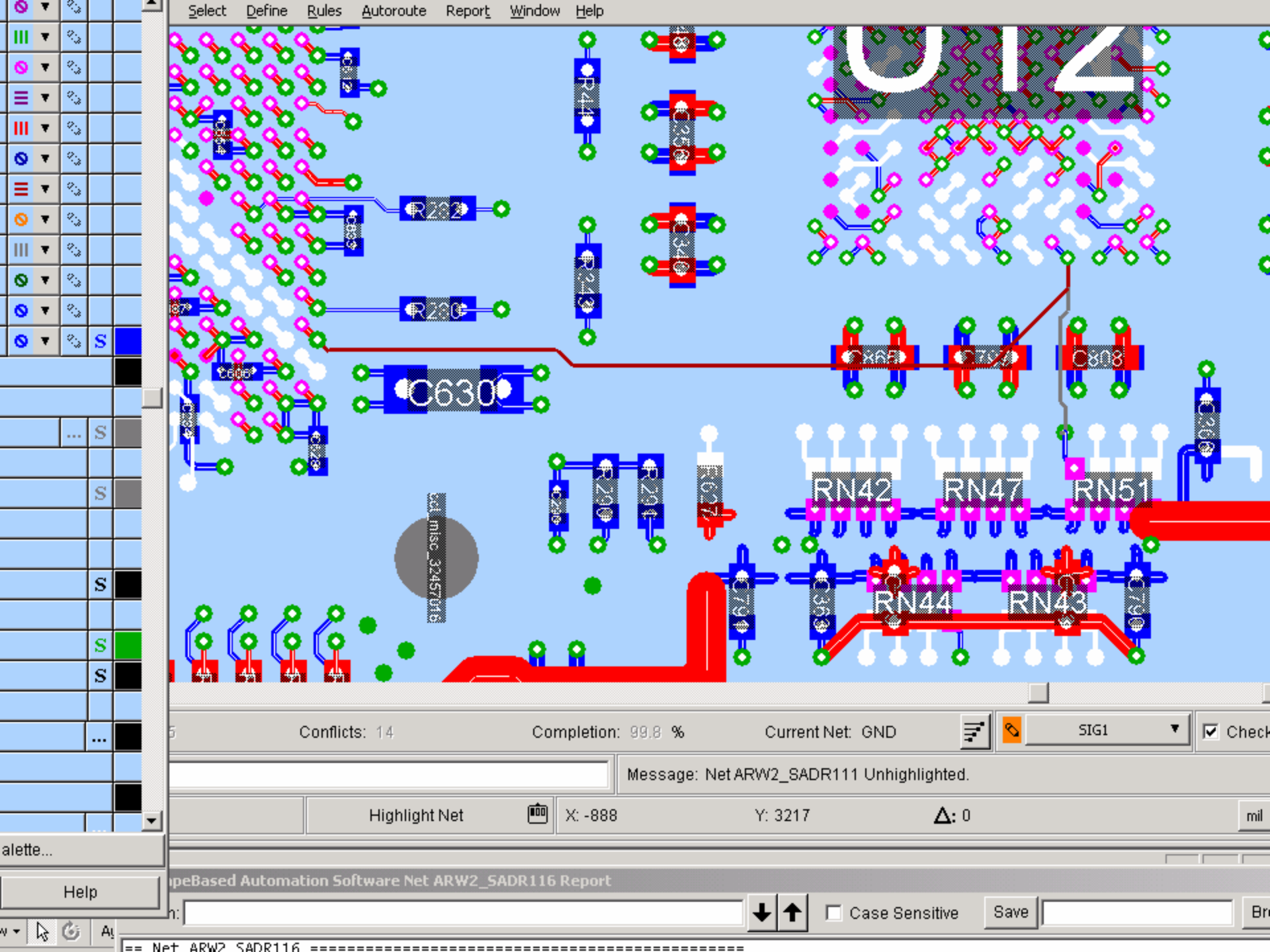
Ways to lure Specctra back: (Nursing the run)

- Check it early in the run to see it that got it right:
- You can avoid wasting time on a worthless run and find a solution sooner rather than later.
  - To do this Pause the router
  - Turn visibility off on all routing layers leaving only top and bottom visible.
  - Turn labels on.
  - Use view highlight class selecting a class with order and be clear in you mind what it should be.
  - All the pins in the class will be white (my colour scheme the default original)
  - Zoom to include the nets

When Specctra goes AWOL on ORDERS

Ways to lure Specctra back: (Nursing the run)

- You can avoid wasting time on a worthless run and find a solution sooner rather than later. (continued)
  - Now pick one of the white pins in view highlight net mode.
  - The traces of just that net become visible so you can see if it is following the required sequence.
  - If it is, do a repaint - the traces disappear - go on to the next.
  - If it is wrong pick it again to turn white marking it as wrong and go on to the next.
  - Sounds cumbersome but with a little practice you can determine quite quickly.
  - **Whether you have problems, none, a few or a disaster.**


Select
Define
Rules
Autoroute
Report
Window
Help
C630
RN42
RN47
RN51
RN44
RN43
C808
Conflicts: 14
Completion: 99.8 %
Current Net: GND
SIG1
Message: Net ARW2_SADR111 Unhighlighted.
Highlight Net
X: -888
Y: 3217
Δ: 0
mil
Help
Case Sensitive
Save

When Specctra goes AWOL on ORDERS

Ways to lure Specctra back: (Nursing the run)

- If you have none - continue the run.
- If you have a few – your call.
- If you have a disaster -- accept my condolences.
- At least you didn't build it.

When Specctra goes AWOL on ORDERS

Ways to lure Specctra back: (final bed check)

- When the run finishes (in idle state) all ordered nets should be checked and if a confirmation report is required (also a handy thing in a tag team) then:
  - Select all the ordered nets and report network by name to a text file that you text edit to mark ok or err adding the actual order and required order to those in error as you go. If the stub is close you might record it to negotiate a waver. Stub Length in net report – paste it across.
- Now to use the technology editor in a way the developers never anticipated.
- Note all the ordered nets and only the ordered nets are still selected.

When Specctra goes AWOL on ORDERS

Be sure Specctra remained back: (final bed check)

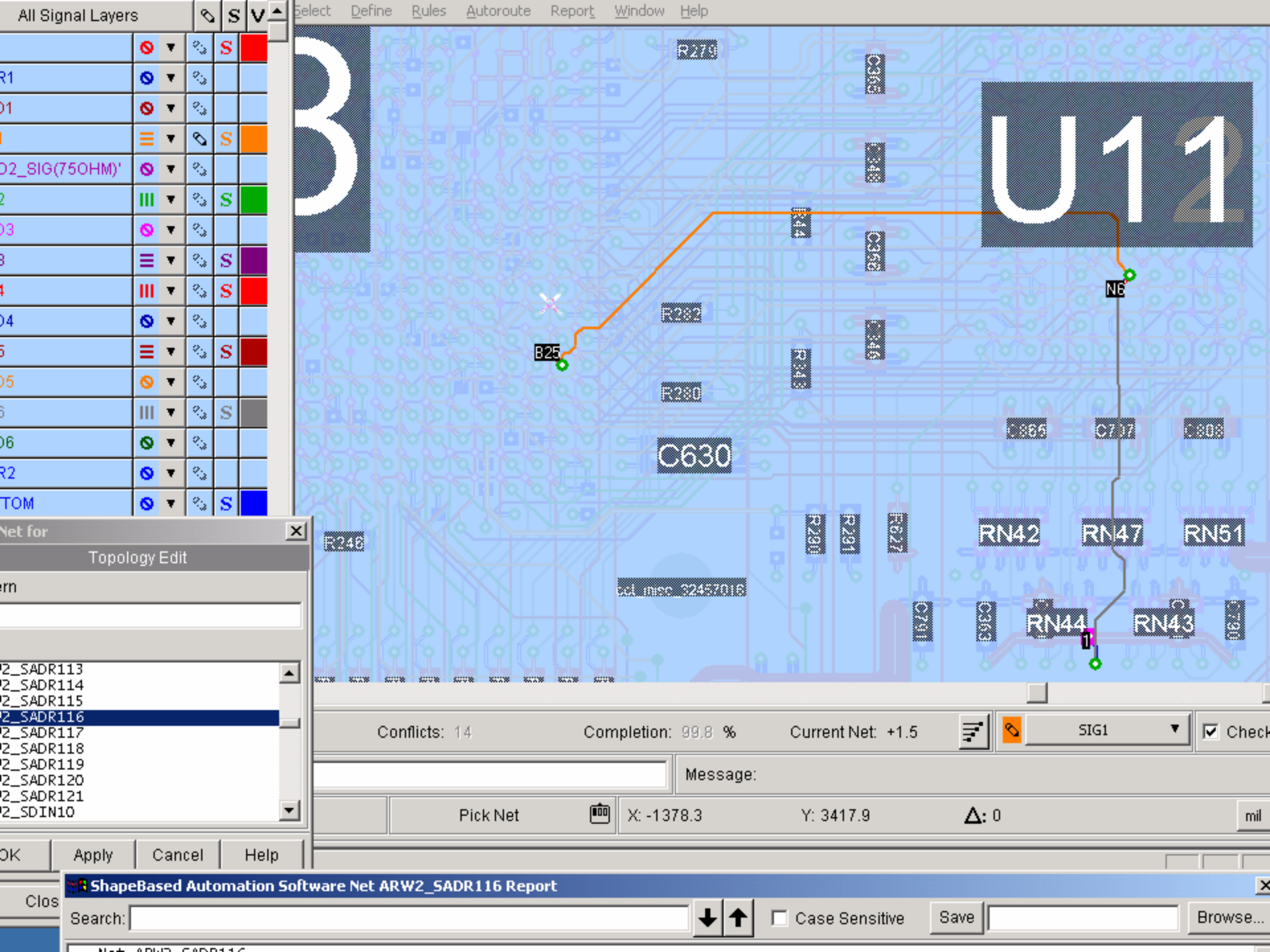
- Using the technology editor to check 5 or (10 when you have had some practice) nets per minute.
  - Mouse 3 --Topology editing menu
  - Alternate topology editing --set shadow very low (button to the far left)
  - Click by list for pick net
  - Window pops with list use pattern or scroll to the net you want. -- Click it
  - Click apply (will highlight and fit the net its pins and you can pan zoom and scroll as necessary)

When Specctra goes AWOL on ORDERS

Be sure Specctra remained back: (final bed check)

- You need a reference for what the order should be:
  - I name ordered sets as classes with the order in the class name then reference the class report for nets in class.
    - `define (class QDR_U11_U12_U8_R (topology (comp_order U11 U13 U8 R%)))`
    - `define (class QDR_U8_U11_U12_R (topology (comp_order U8 U11 U12 R%)))`
    - `define (net ARW2_RE0 (comp_order U8 U11 R328 ))`
  - Delete or mark the net on your net list as appropriate.
- Click and apply the next net etc. etc.
- Again it sounds cumbersome compared to just generating a report but at about 5 seconds each, that's about 7 hundred per hour.

AND YOU KNOW THEY ARE RIGHT!


All Signal Layers
Select Define Rules Autoroute Report Window Help
U11
C630
RN42
RN47
RN51
RN44
RN43
B25
N6
Topology Edit
ARW2_SADR113
ARW2_SADR114
ARW2_SADR115
ARW2_SADR116
ARW2_SADR117
ARW2_SADR118
ARW2_SADR119
ARW2_SADR120
ARW2_SADR121
ARW2_SDIN10
OK
Apply
Cancel
Help
Conflicts: 14
Completion: 99.8 %
Current Net: +1.5
SIG1
Message:
Pick Net
X: -1378.3
Y: 3417.9
Δ: 0
mil
ShapeBased Automation Software Net ARW2_SADR116 Report
Search:
Case Sensitive
Save
Browse...

When Specctra Follows ORDERS

- Avoiding being run over by a BUS.
- On occasion the requirement comes through as this class is to routed as a daisy chain.
  - What may be omitted is that this class is a bus and therefore all members must be daisy chained in the same order.
  - If you just specify daisy at the class level, Specctra will (as it should) simply determine the shortest daisy for each net which will not give the same order for some members depending on placement. → functional failure
  - For bus daisy chain use the following unambiguous syntax:
    - `rule class uxyzr (tjunction off)`
    - `rule class uxyzr (max_stub 200)`
    - `define (class uxyz (topology (comp_order Ux Uy Uz R*)))`

Some Things DO NOT work WELL

REGIONS:

- **The definition a region of creates a discontinuity along its boundary that SEVERELY CRIPPLES both movement by the AUTO ROUTER and in INTERACTIVE EDITING. Pairs tell you over and over that they don't work for them.**

VIRTUAL PINS:

- **Release 15 rewrite compatibility could be an issue.**

BUNDLES

- **A defined SET of N nets, that go like a huge pair.**
- **All of the problems outlined for diff. Pairs with their impact multiplied by N.**
- **Release 15 serious work on pairs could benefit bundles later.**

PAIRS

- **Release 15 serious work on pairs .**

Some Things ARE NOT THERE NOW

- **TRUE 45 DEGREE AUTO ROUTING.**
  - Can be emulated sort of with a staged sequence of miter commands and cleanup effort at the end.
  - CCTUG Provided a user requirement spec Jan 01 2001.
- **WYSIWYG copper planes (polygons) on signal routing layers cannot be perforated by vias.**
  - Release 15
- **TANDEM, BROAD SIDE, OVER AND UNDER, ADJACENT LAYER PAIRS, STRIP LINE PAIRS**
  - Release 15 maybe ???? PART OF PAIRS REVISION?

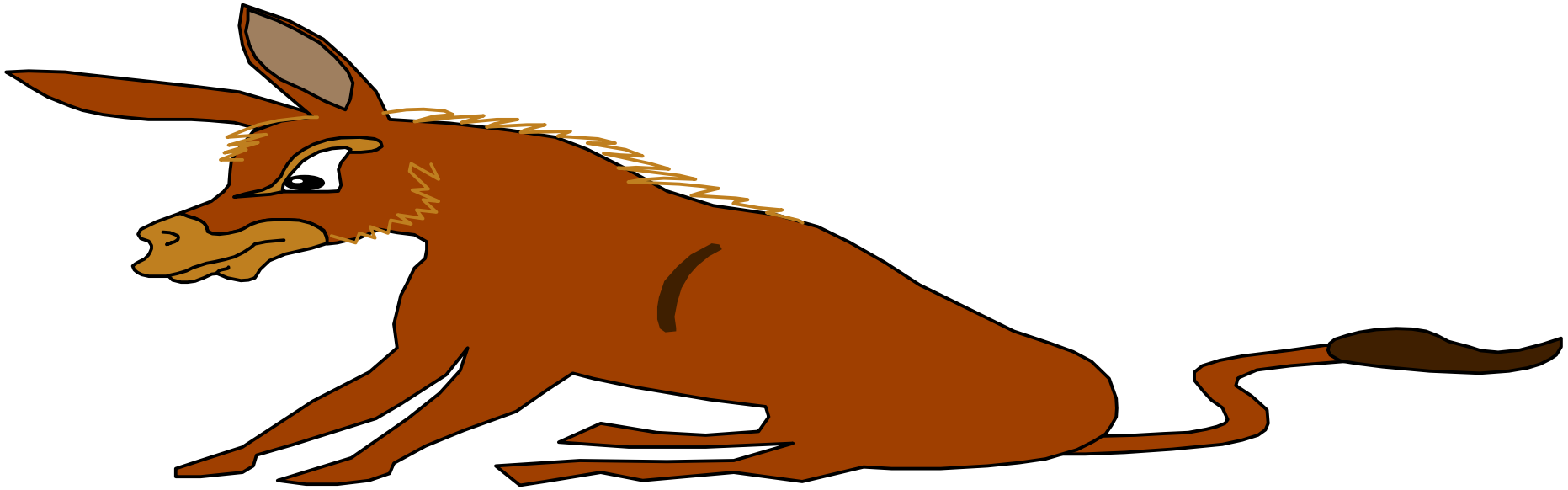
Some Things ARE NOT THERE NOW

- **CLASSES ASSIGNED TO EITHER OR LAYER SETS.**
  - **THIS NET SET MUST ALL GO ON ANY ONE OF THE LAYER PAIRS DEFINED.**
  - **Release 15**
- **KEEP OUTS AND KEEP INS FOR CLASSES NETS GROUPS ETC.**
  - **A NEEDED COMMINICATION CHANNEL BETWEEN USERS AND THE CORE ALGOITHMS.**
  - **SHOULD BE ABLE TO DO SOME OF THE THINGS REGIONS AND FENCES TRIED TO DO IN THE SIMPLER DESIGNS OF THE PAST.**
  - **HIGH SPEED SIGNAL INTEGRITY.**

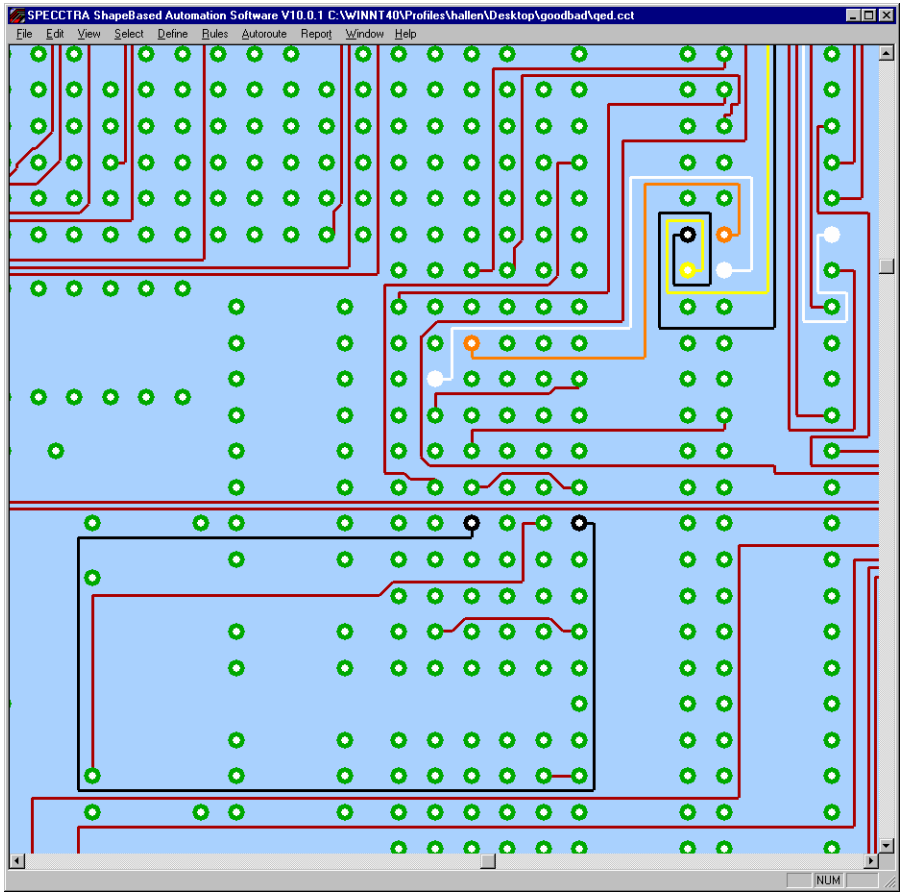
SOME BASIC PRINCIPLES

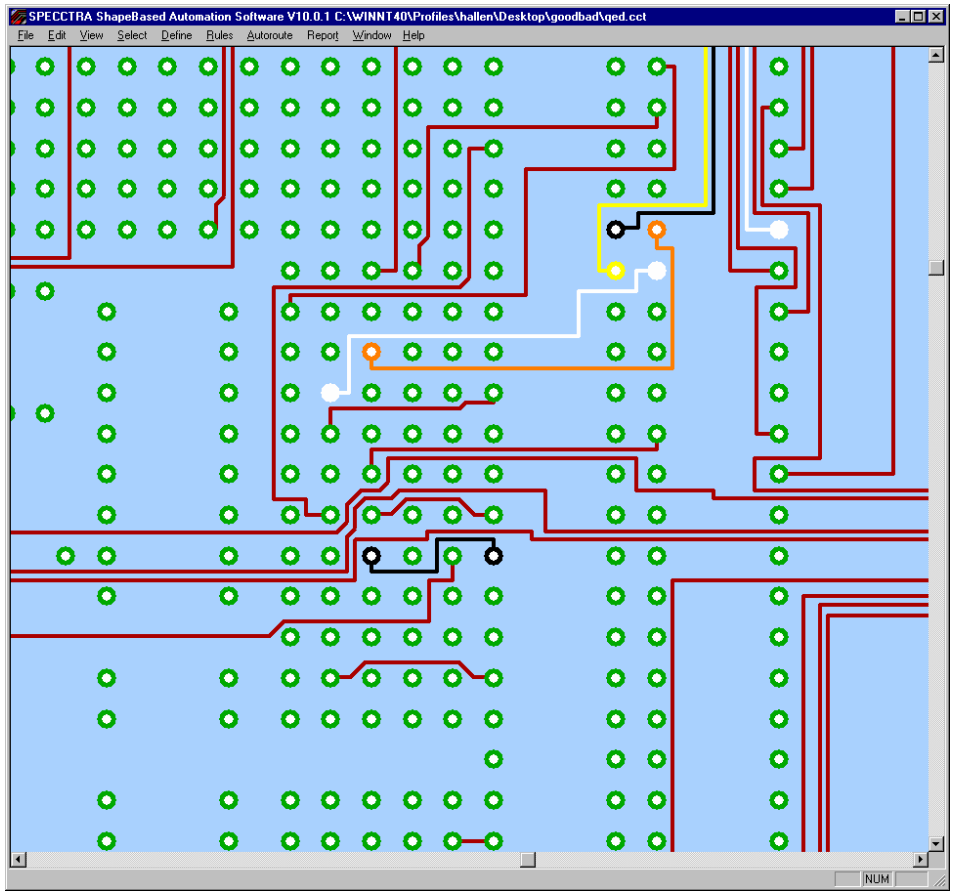
SPECCTRA OPERATES ON “WORK TO RULE”

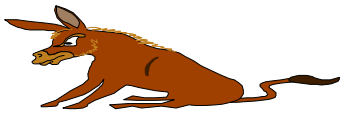
- **If NO UNCONNECTS & NO RULE VIOLATIONS then Specctra is ALL DONE here!**
- **NOT a “GET IT RIGHT the FIRST TIME” thing.**
- **Works on CONTINUOUS IMPROVEMENT.**
- **Get the router to do the BEST IT CAN -- then FIX UP what it falls short on to the required level of perfection.**
- **THE BEST OF BOTH WORLDS!**



HAVE TO MAKE WORK TO RULE WORK FOR US

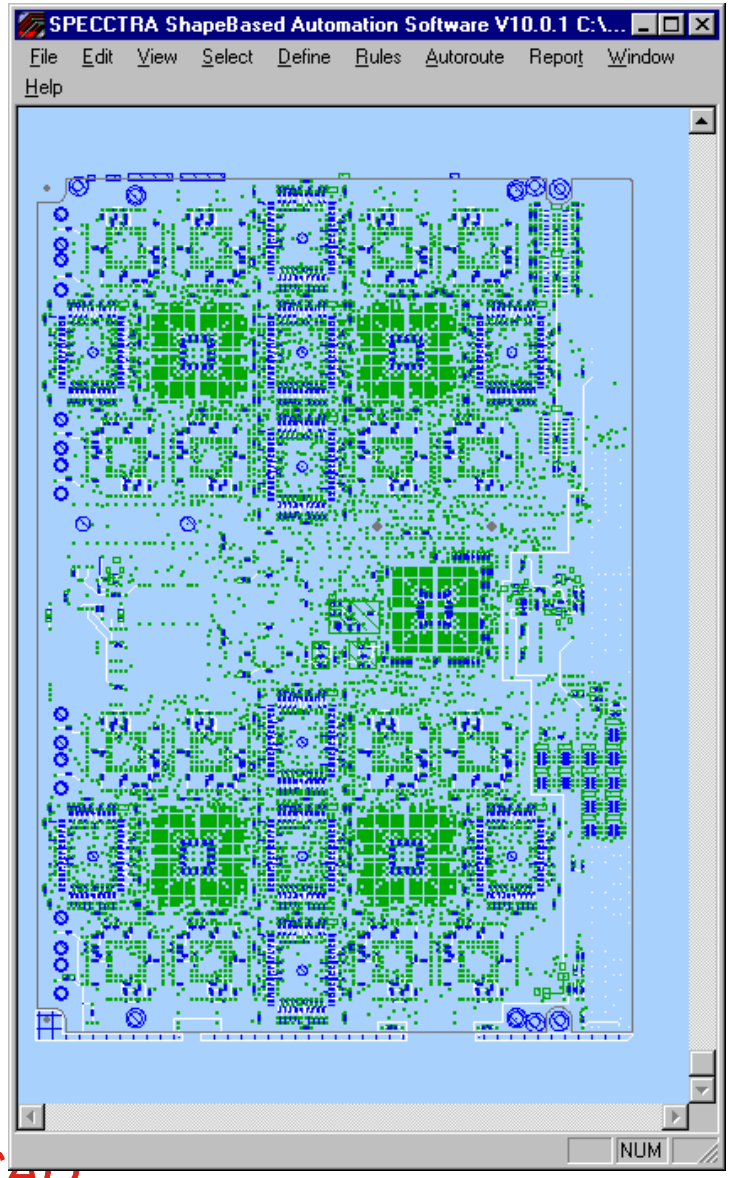




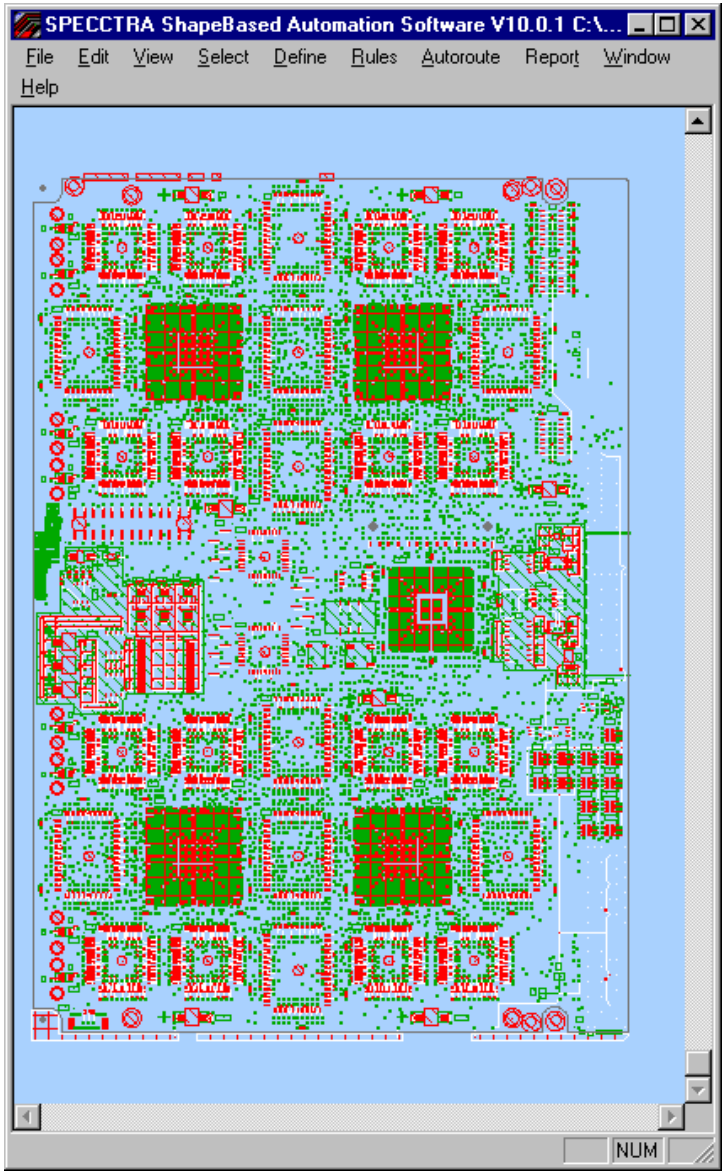


Progress SPECCTRA Related

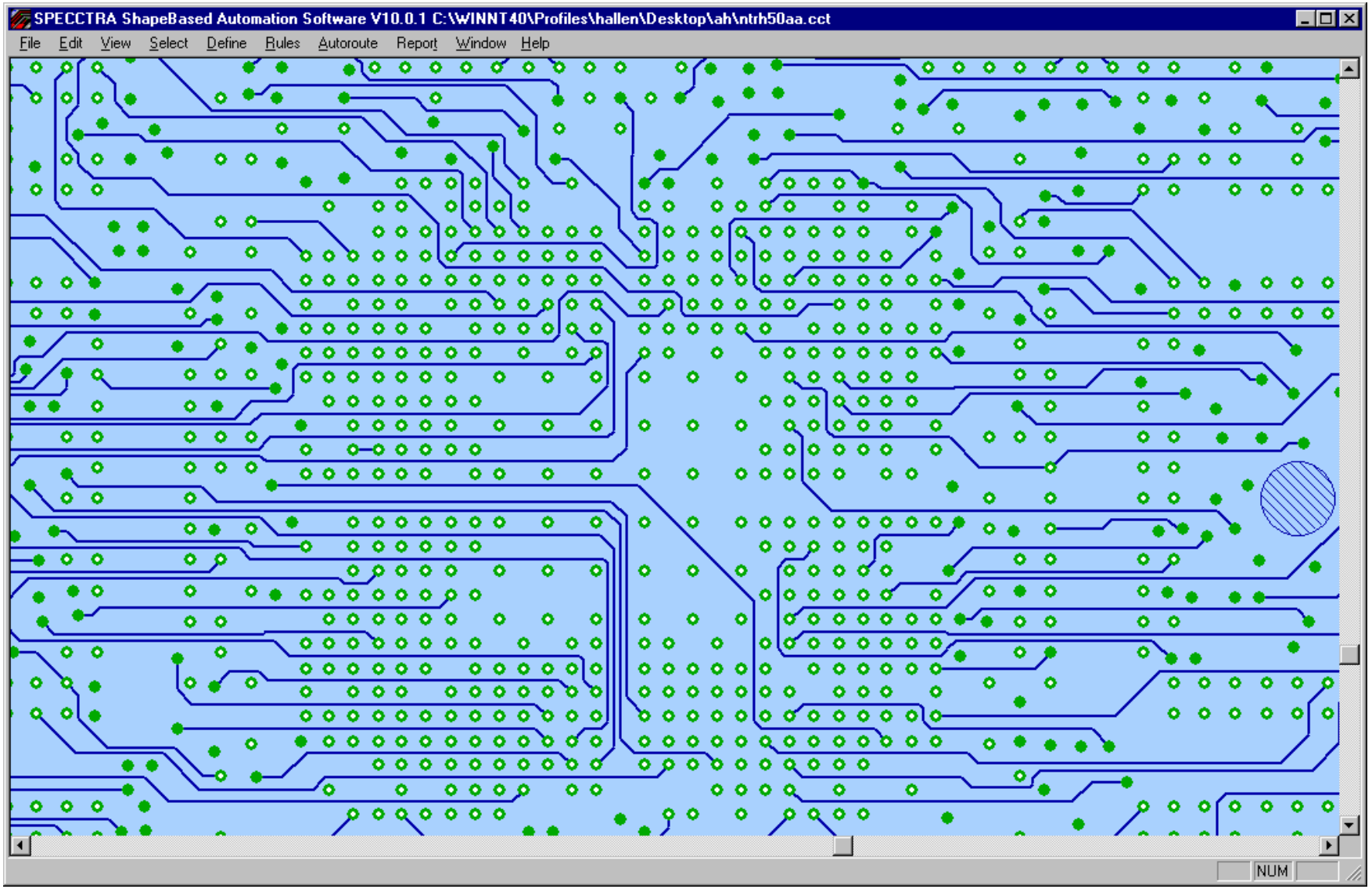
BOTTOM



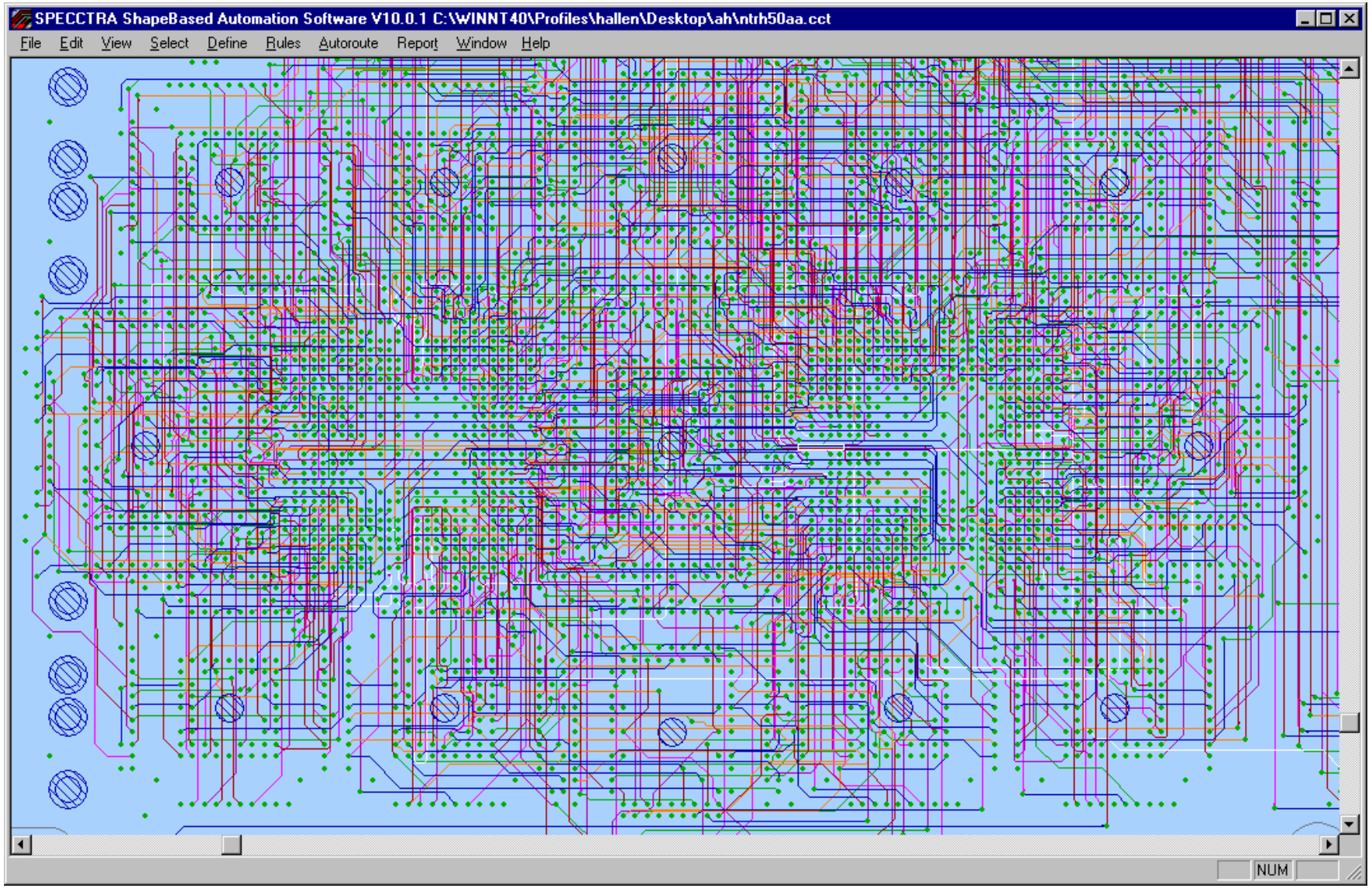
TOP



Progress SPECCTRA Related



Progress SPECCTRA Related



Nets = 2064 Connections =6297

#Overall **Routing Time 12:51:30 hook up 2:47:36**

That was last year. Holding the performance

Line on software new hardware goes 8 hours now!

#WIRING STATISTICS PCB Area= 56.099 **EIC=675**

Area/EIC= 0.083 Components=936 SMDs=930

Signal Layers=8 Power Layers=4 Wire

Junctions=381, at vias=381 Total Vias=8631

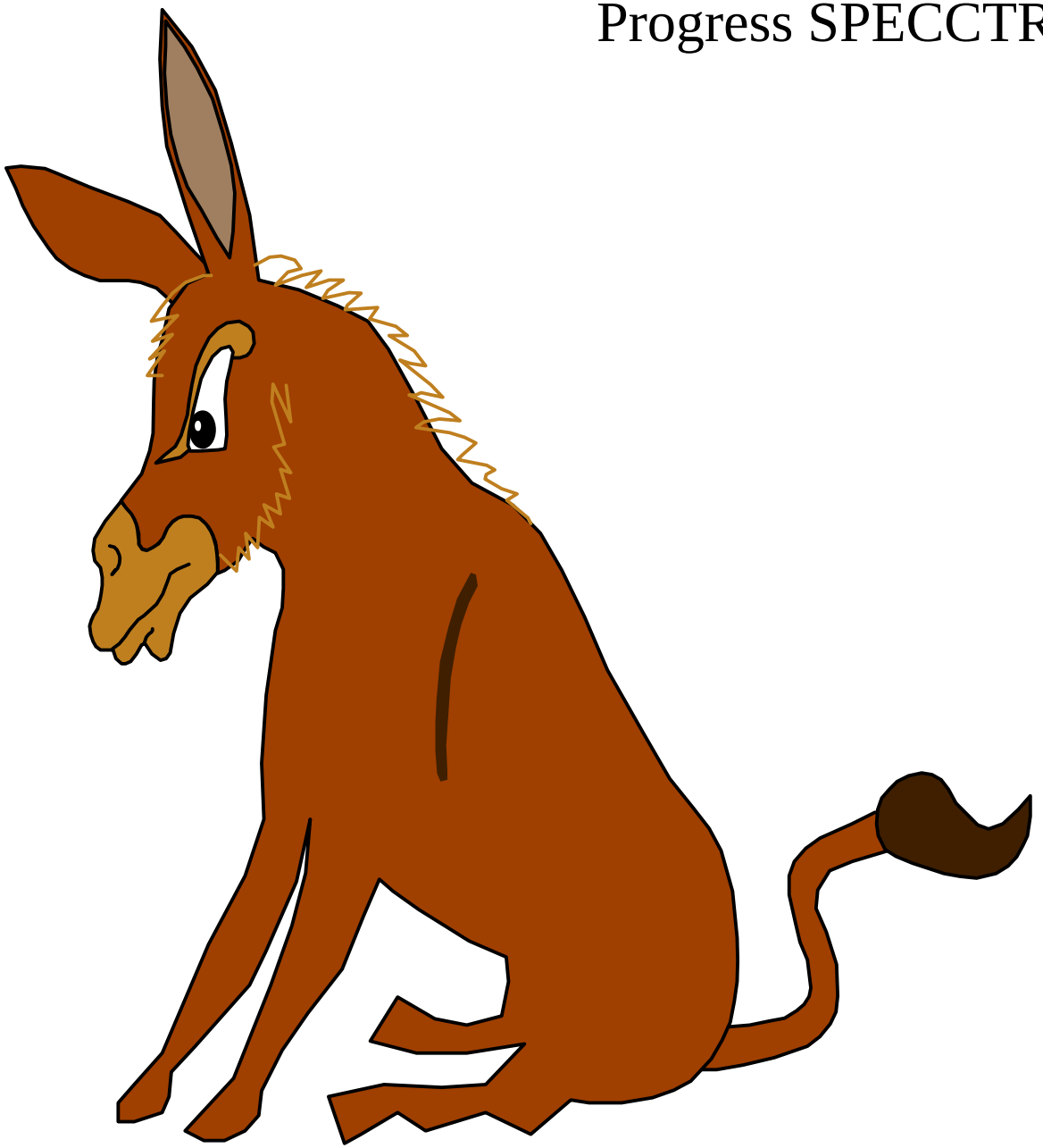
Conflicts=0 Crossovers=0, Clearances=0,

Crosstalk=0, Length=0

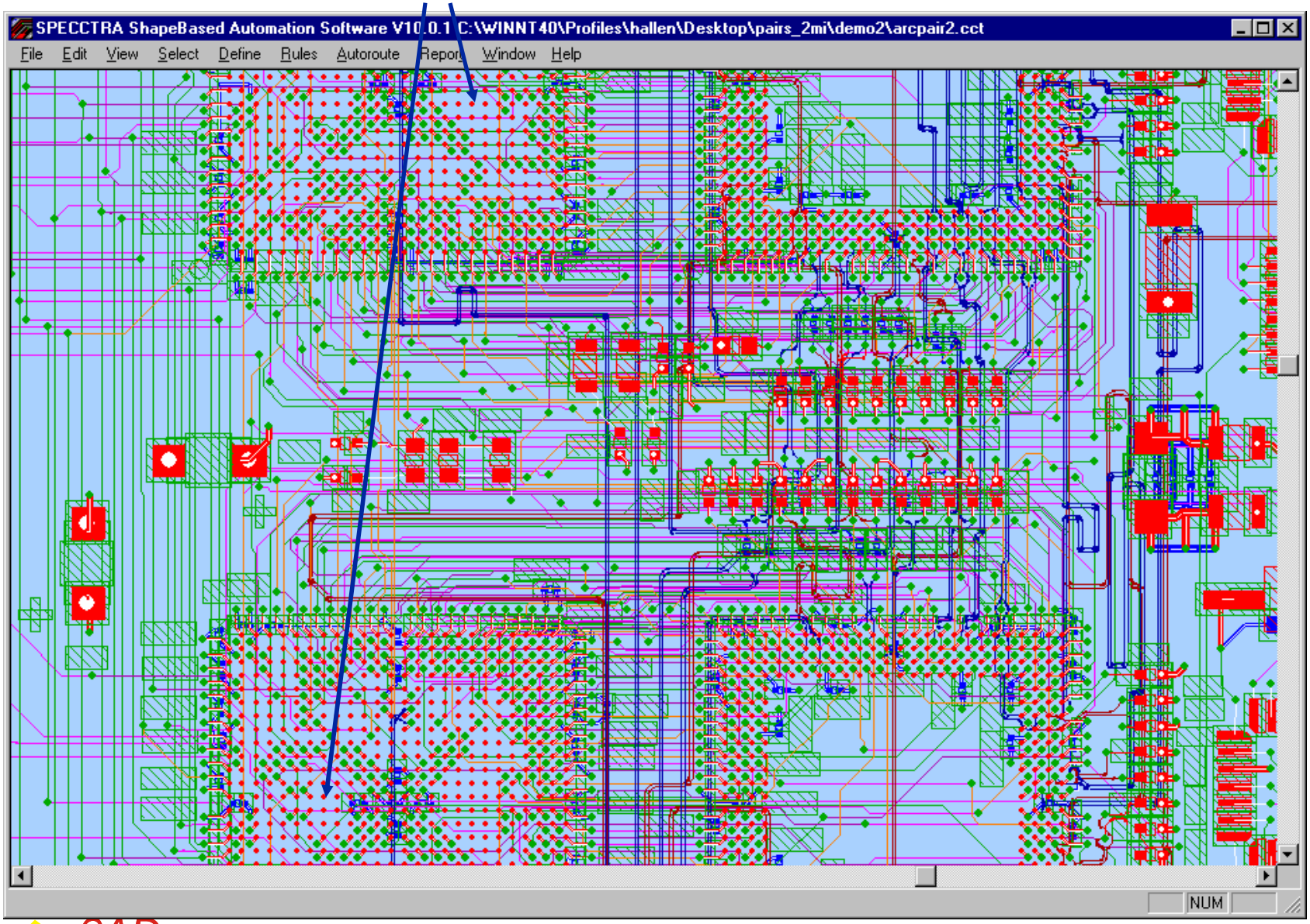
Manhattan length=4024.106

Routed length= 3903.073

Ratio Actual / Manhattan= 0.9699

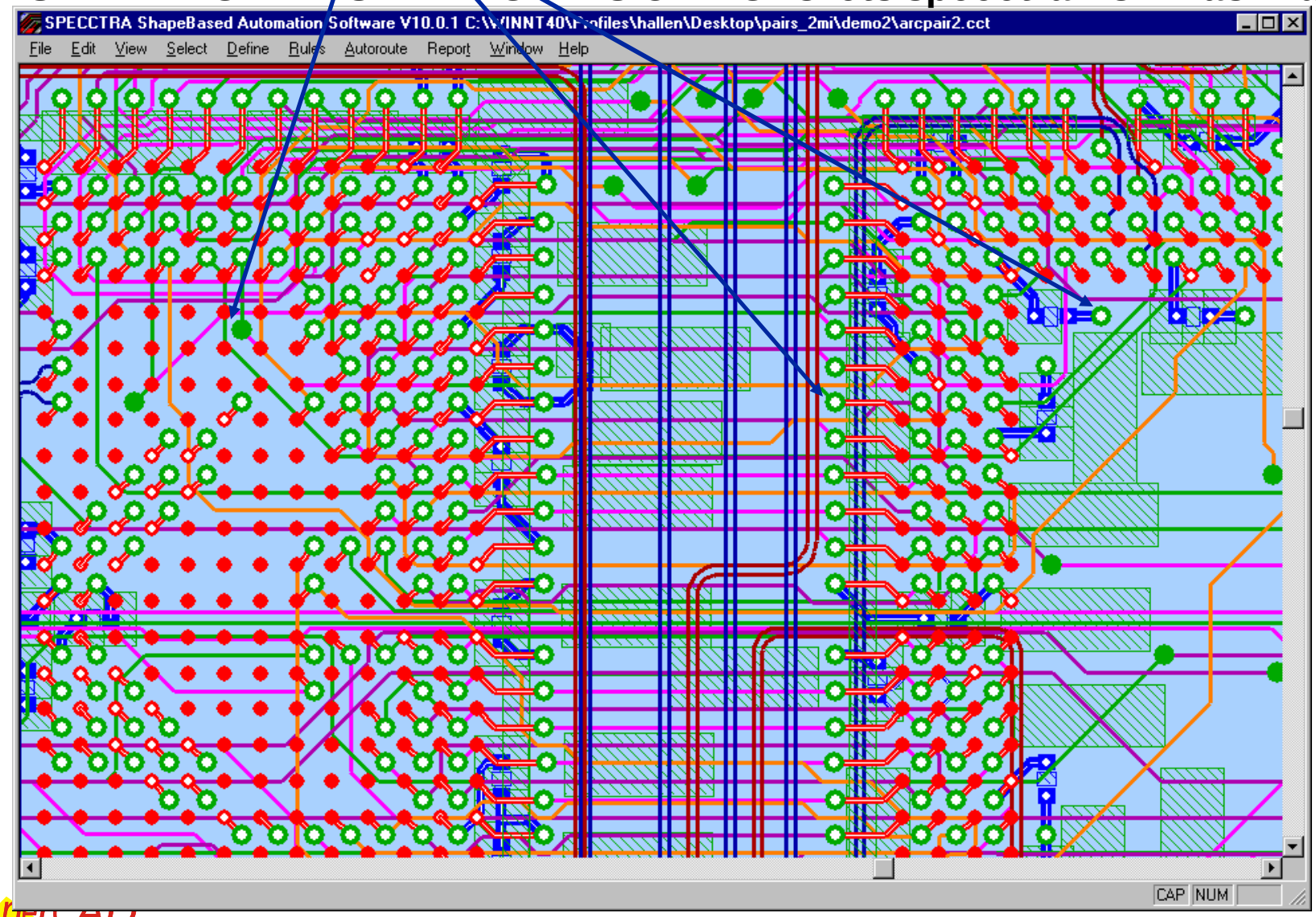


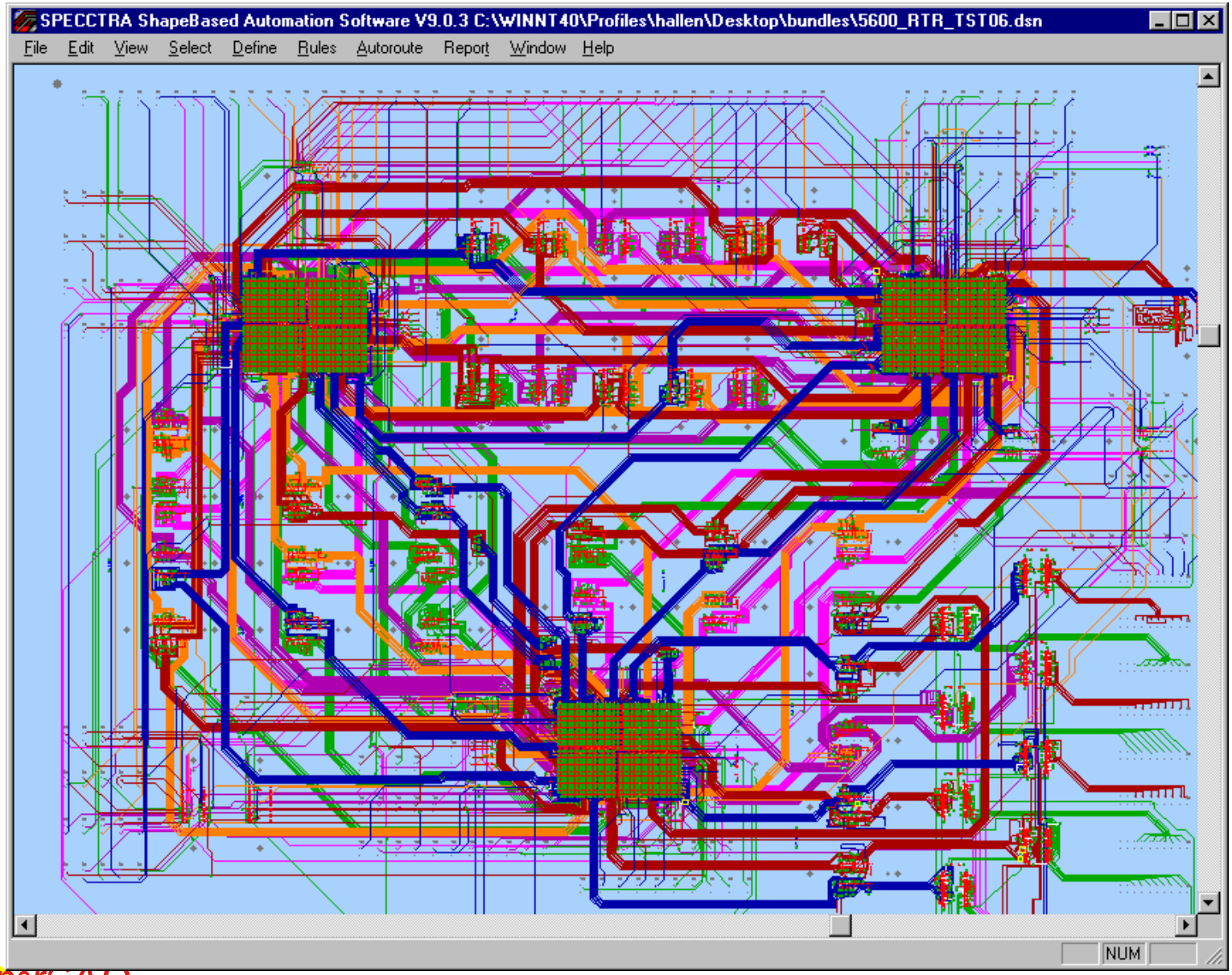
BGA Unused pins via's omitted



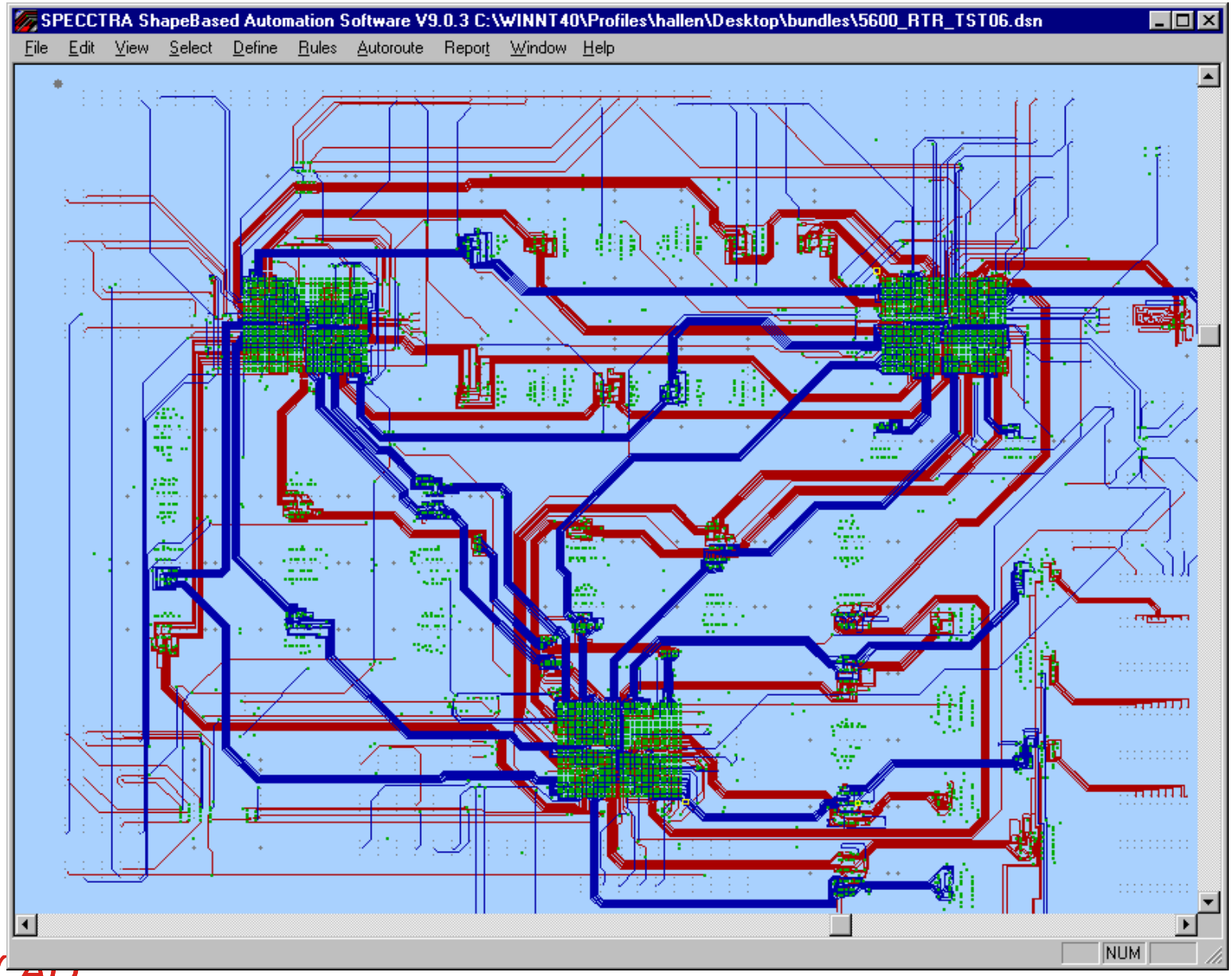
PRE-ROUTE VIA ALIGNMENT IS CRITICAL

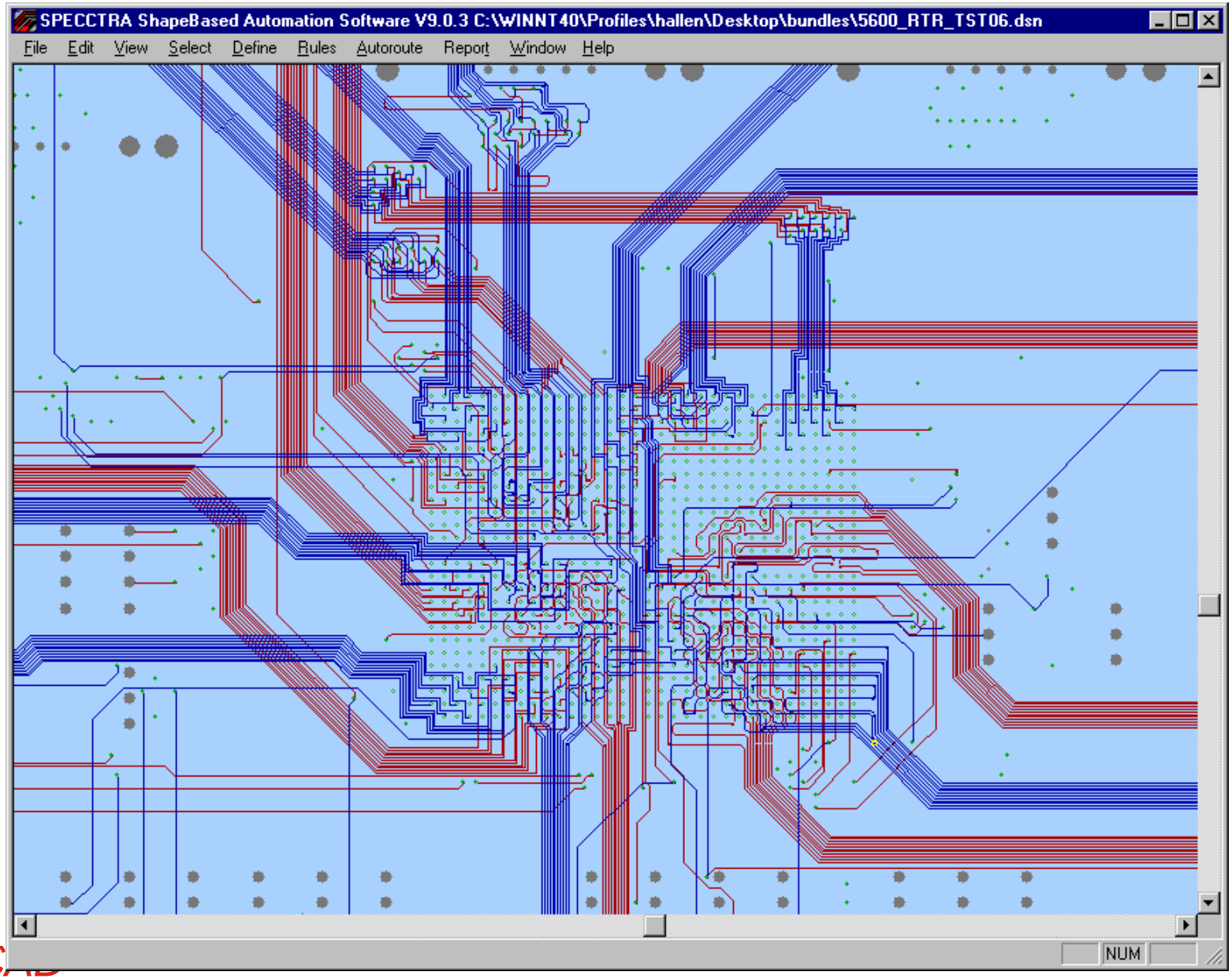
STRIPPING AND SHARING VIAS ON BGAs lets specctra PUT vias in array




SPECCTRA ShapeBased Automation Software V9.0.3 C:\WINNT40\Profiles\hallen\Desktop\bundles\5600_RTR_TST06.dsn
File Edit View Select Define Rules Autoroute Report Window Help
NUM

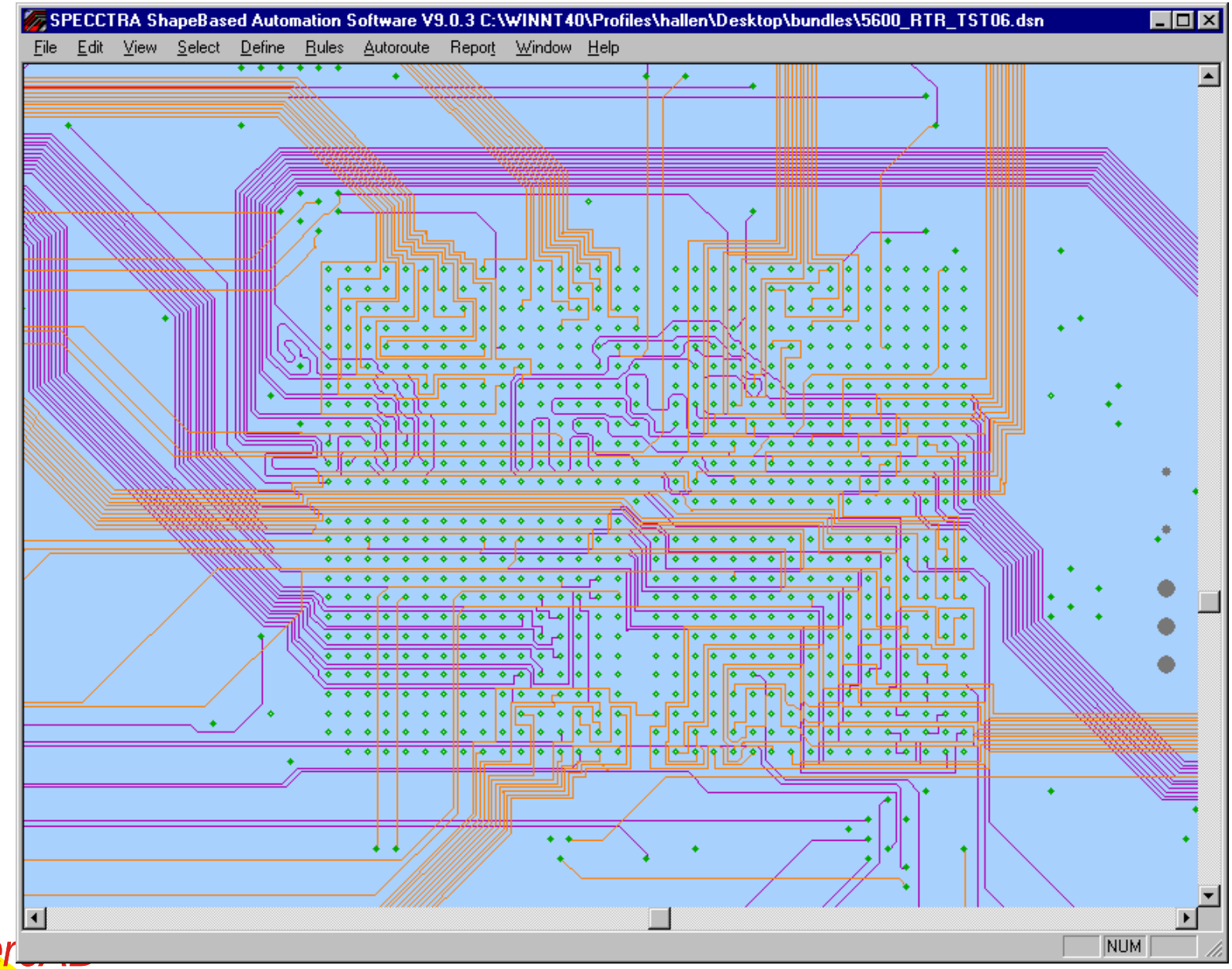
BUNDLES


SPECCTRA ShapeBased Automation Software V9.0.3 C:\WINNT40\Profiles\hallen\Desktop\bundles\5600_RTR_TST06.dsn
File Edit View Select Define Rules Autoroute Report Window Help
NUM

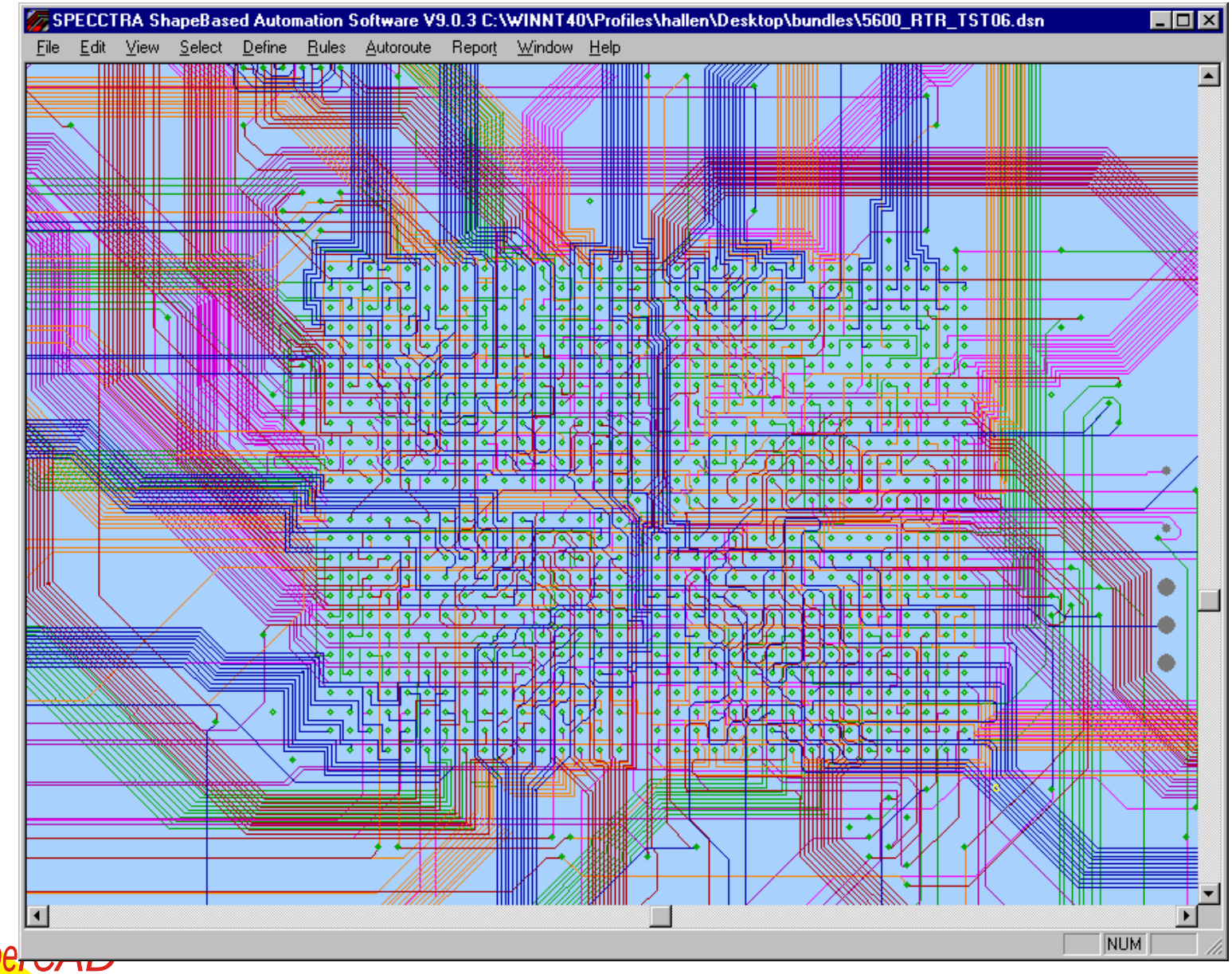

SPECCTRA ShapeBased Automation Software V9.0.3 C:\WINNT40\Profiles\hallen\Desktop\bundles\5600_RTR_TST06.dsn
File Edit View Select Define Rules Autoroute Report Window Help
NUM

BUNDLES

Progress SPECCTRA Related



BUNDLES


SPECCTRA ShapeBased Automation Software V9.0.3 C:\WINNT40\Profiles\hallen\Desktop\bundles\5600_RTR_TST06.dsn
File Edit View Select Define Rules Autoroute Report Window Help
NUM


SPECCTRA ShapeBased Automation Software V9.0.3 C:\WINNT40\Profiles\hallen\Desktop\bundles\5600_RTR_TST06.dsn
File Edit View Select Define Rules Autoroute Report Window Help
NUM