## DesignCon 2003
## Abstract

Title: Practical Guidelines for the implementation of back drilling plated through hole vias in multi-gigabit board applications

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### Tom Cohen

Tom is currently a principle mechanical engineer in the New Product Development group. His current activities include the design and analysis of high speed next generation products. During Tom's 20 years of industry experience he has received numerous interconnect patents and has authored several papers. Tom has a BS degree in Mechanical Engineering from the University of Pittsburgh.

### Abstract:

In copper board to board applications, data rates of 2.5 Gb/s are common. Recently there have been numerous efforts to boost single channel data rates to and beyond the 10 Gb/s range. These channels can be broken into segments comprised of the device, package effects, board laminate material, high speed connectors, and the launches into and back out of the interior layers of the printed circuit boards or via's. This paper will focus on the PCB launch, specifically a technique referred to as back drilling. It has been shown in previous DesignCon papers that by back drilling the via, the launch impedance is improved by reducing via capacitance and more importantly the launch resonance effect is mitigated. In thick boards, such as backplanes, S21 measurements have shown a well defined notch at around 5 GHz where very little power gets through because the stub behaves like an unterminated transmission line. Other high speed applications have considered back drilling such as BGA patterns and coaxial launches. The effect of a drilled via applies equally to surface mount terminations where a drilled through hole is used to connect to inner layers deep in the board. This paper will address some unanswered questions which have been raised by designers on the implications of using this technique. Electrically, measurements will provide design guidelines for improved frequency response as a function of stub length. Via diameter, antipad diameter, and board laminate material will also be considered. Mechanically, long term reliability of a back drilled via structure will be looked at for CAF growth and compliant pin termination and repair. Accelerated life testing will stress the back drilled holes to look for delamination and other detrimental effects. The producability of the printed circuit boards will be analysed in the area's of required overdrill diameter, z axis depth accuracy, and a cost estimation.

### Back Drilling Overview

- Electrical effects
- Process implications
- Reliability Testing
- Conclusion

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## Introduction

Transport data rates of 3.125 Gb/s are now commonplace in board-to-board applications. As data rates increase to 5, 6.25 or 10 Gb/s the entire channel topography will need to be re-examined. A typical transmission channel includes signal traces, connectors, and plated through hole vias. New connectors are entering the market with better impedance matching and improved shielding techniques to accommodate the sharper rise times associated with the faster data rates. Likewise laminate suppliers continue to develop new board materials with lower loss tangents to reduce the signal attenuation due to laminate loss. Using equalization circuits and signal pre-emphasis, device suppliers are driving solutions to improve signal fidelity at increased data rates.

A piece of the transmission path which cannot be neglected, is the plated through hole or via. Plated through holes or PTH's are a means to transport signals into interior layers of a multi layer PC board. PTH vias are used in this way under the pad array of the device package, and in the launch of separable connector interface into boards. The PTH is common to various device packages such as a ball grid array (BGA) and connector types including press fit and surface mount right angle board-to-board, mezzanine and cable connectors. In the case of a typical backplane system, the signal passes through at least six vias or PTH's while traveling from driver to receiver, and the board thickness

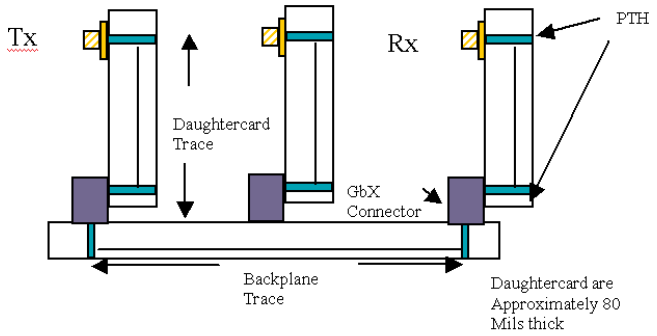
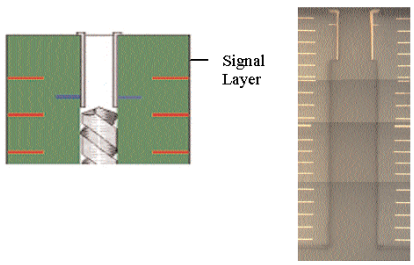



Figure 1 – Typical signal path

in such a system can result in relatively long plated through holes.

The PTH portion of the signal path becomes more "visible" to the signal as increased frequency content is needed to produce sharp rise and fall times of the digital pulse. The focus of this paper will be on a technique commonly referred to as back drilling or counter boring of the printed circuit board PTH. Included in this study will be the electrical effect, the process implications including a cost model and results of long term reliability testing.

**Back drilling**
**Removing the unused portion of PTH**



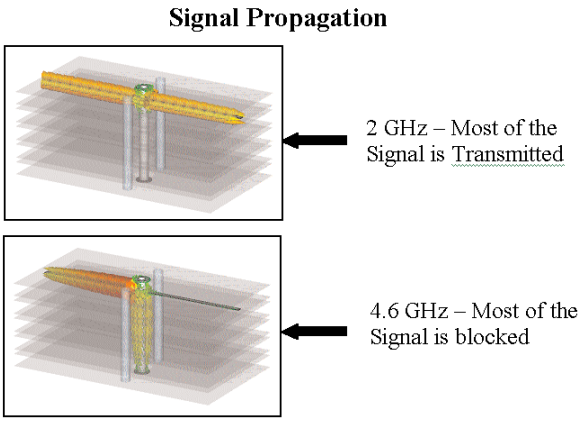

## Background

The actual rise time and frequency content of digital pulses may vary. The frequency spectrum of a PRBS digital data stream typically consists of bands centered around a fundamental and its odd harmonics. The fundamental frequency of the spectrum occurs at one half of the data rate. At 2.5Gbits/sec, this means that the fundamental frequency would occur around 1.25GHz with some contribution around the third (3.75 GHz) and fifth (6.25Ghz) harmonics. The transmission vs. frequency response will be shown for various via geometries, together with eye patterns which incorporate the effects of the higher harmonics. A PTH or through via joining a surface pad or connector to an inner layer strip line trace, can behave as a parasitic element or transmission line discontinuity. It acts as a notch filter centered around a frequency primarily determined by the unused portion of the hole, sometimes referred to as a resonant stub. As a signal transitions into a plated through hole, some of the energy is reflected back to the source from the impedance discontinuity. The remaining energy proceeds through the via. The energy that is transitioning through the plated through hole uses the hole as a transmission line element whose parameters are defined by the physical dimensions of the structure (pad size, anti-pad size, etc.) It then reaches an impedance matched stripline layer. Some of the energy is transmitted into this layer and some continues to travel down the remaining via. Any portion of the plated through hole below the exiting stripline layer can be looked at as an open transmission element referred to as a stub.

The energy that passes the exiting stripline layer proceeds to the end of the stub and encounters an open circuit, and it is reflected back towards the source or converted to radiation. At low frequencies a PTH element could simply be modeled as a lumped capacitor. At higher frequencies the round trip delay for this PTH element approaches the signal rise time and the simple capacitive approximation no longer holds. The length of the stub could be over 8mm in a backplane. As an example, in our 0.220" thick test board, the maximum stub was 5.0mm. The delay of pure FR4 is approximately

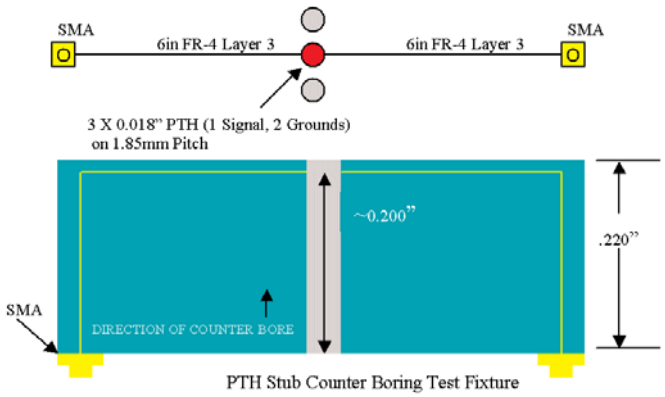
7ps/mm or 175ps/inch. The calculated delay from the open end of the stub to the strip line layer is approximately 38ps. The calculated quarter wavelength frequency of this open stub element resembling an antenna is approximately 7 GHz. The actual observed frequency is always somewhat lower due to excess fringing capacitance and other effects from the details of the structure. For example, in the test board shown in Figure 2, the notch was measured at 4.5Ghz.

If the notch created by this resonance occurs at a frequency, which is close to the fundamental frequency, only a percentage of the transmitted signal would make it past the filter created by the stub.



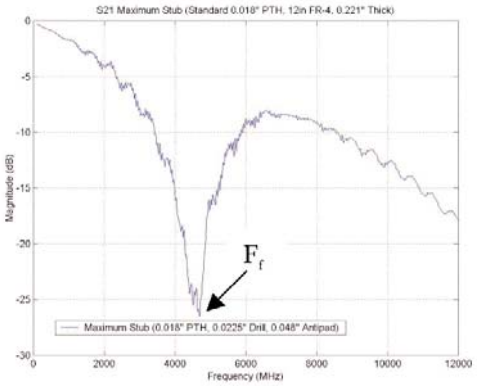

### Experimental Measurements

A simple single PTH test fixture was created to focus on the PTH effect independent of any connector or device package as shown in Figure 2. Figure 3 shows the measurement of a 0.018" finished hole size via. in a 0.220" thick FR4 PCB test fixture where the stub is 0.200" (figure 2.)



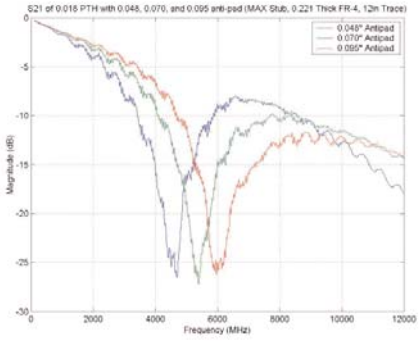

PTH Stub Counter Boring Test Fixture
Figure 2

In order to isolate which physical feature could be altered to change or tune the resonant behavior of the via, measurements and simulations were done to determine the variation of this approximate notch frequency (Ff) as a function of the ground plane relief (anti pad), the laminate material, the via diameter, and finally the via stub length.




Notch Frequency
Figure 3

Regarding the anti-pad effects of the test board figure (4), clearances of .048", .070" and .095" diameter ground plane clearances were measured. It could be seen that even increasing the anti-pad diameter to .095" moves the notch up approximately 1.5 GHz, not enough to ensure good transmission over the zero to 6 GHz bandwidth that is required for a 6 Gb/s signal. It should be noted that anti pads of this size could not be used under a BGA, or within a high-density connector footprint.

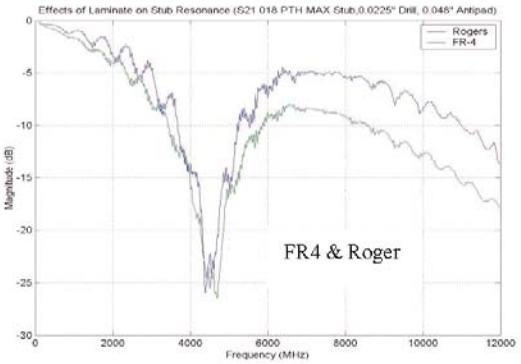



Anti-pad Effect
Figure 4

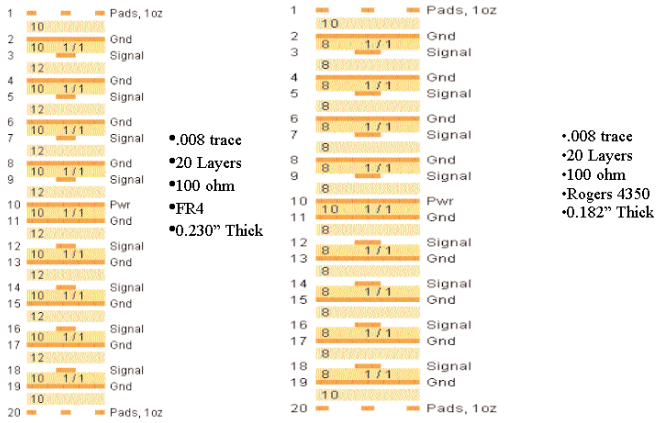
Changing the board laminate material will also affect the notch frequency. As seen in figure 5, Ff only moves a few hundred MHz due to laminate alone when the via diameter and length are held constant. This is primarily due to the change in electrical length of the via due to a change in dielectric constant where the propagation velocity Vp = c/sqrt (Er), where Er is the dielectric constant of the medium and c is the speed of light.

By changing to a laminate with a lower dielectric constant, you will have a larger effect on notch frequency due to the reduced board thickness. For Example, a 20 signal layer board with .008" traces impedance

matched to 100 Ohm would be .230 thick in FR4 and .182" thick in a laminate with Er=3.2. See Figure 6. This length effect will be treated separately.



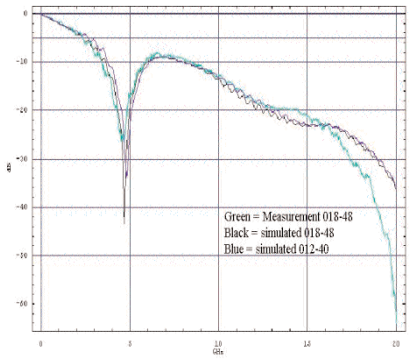

Laminate Effect
FR4 and Rogers 4350 with .200" remaining
Figure 5




Sample Stack Ups
Figure 6

The notch frequency Ff was then studied in relationship to PTH diameter while holding the other variables constant. In this case a combination of measurements and simulations were needed to limit the number of test fixtures required. Simulation was done using finite difference time domain (FDTD) full wave solver by Remcom, Inc. Correlation of this simulation tool to the original test fixture is shown in Figure 7.

This figure contains measured values for a .018 via, and simulations for .012, and .018 vias. The simulated notches are sharper because dielectric and conductor losses were neglected. Although the via diameter has the effect of moving Ff by approximately 200 MHz from the minimum to maximum via studied, this change by itself will not be enough to fully mitigate the stub effect. This implies that simply changing the termination method for a high-speed connection from press fit to surface mount or a pressure interface may not negate the stub effect of the associated PTH or Via.




.018" via – modeled and measured
.012" via - modeled

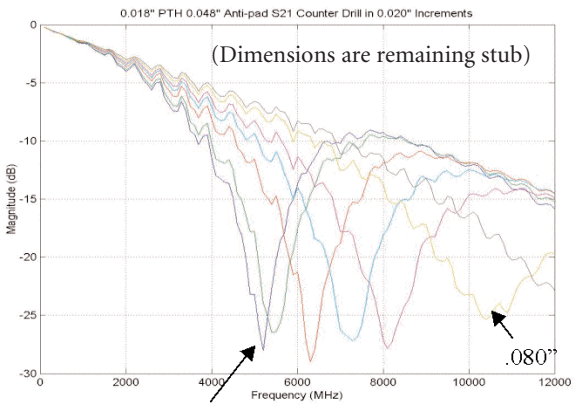
Effect of PTH Diameter
Figure 7

As a first approximation, stub effects are present in any PTH where the combination of material and geometry move the notch into the frequency of interest. Although other variables show some effect the stub notch frequency is primarily a function of its length.

Note: Blind and buried vias are an alternative method which can be used to control the maximum length of a PCB stub. A study of these is beyond the scope of this paper.

Back drilling or counter boring the via is an alternative technique to minimize the stub. A more detailed study of the back drilling process will be discussed in the next section, but back drilling is simply drilling out the unused portion of a via to a controlled depth on the same type of equipment used to initially produce the board.

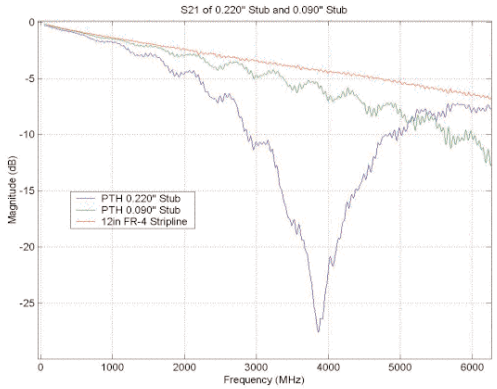
The original test fixture (Figure 2) was back drilled in increments of 0.020" with the resulting successive S21 plots shown in Figure 8 (explicitly counter bore depths of 0.020", 0.040", 0.060", 0.080, 0.100", 0.120", 0.140" leaving stubs of 0.180", 0.160", 0.140, 0.120", 0.100, 0.080" respectively). It can be seen that relatively small increments in stub length have a measurable effect on moving Ff. (Figure 8). A change from .200" to .140 of remaining stub moves Ff out nearly 2 GHz. Similarly, when moving from a .180" stub to a .100" stub, Ff moves out approximately 3 GHz.




Effect of incremental Back drill depth
Figure 8

To understand how this type of information could be used as a first cut design guideline, two examples are shown. Because digital pulse transmission is broadband, containing a number of frequency bands, the single notch frequency Ff is not adequate to determine the effect on a received eye pattern in a system. The width of the notch, or "Q" can also cause excessive attenuation in useable frequency bands. Loss will be looked at in the frequency band of a fundamental frequency up to 2 times the fundamental to account for the notch width.

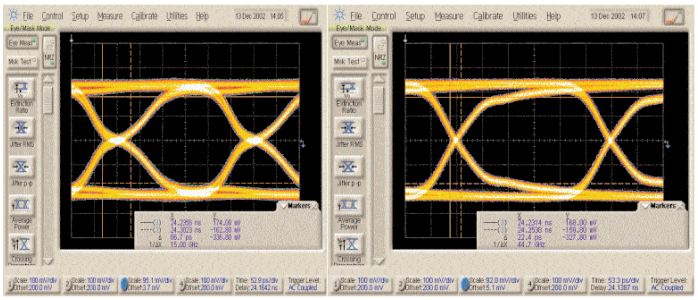
Two examples are shown, one at 3.125Gb/s and one at 6.0 Gb/s. Remaining stub lengths of 0.0220" and 0.090 with a .018" PTH were compared at these rates in a fixture containing 12"of FR4, and 2 SMA's. A 12" FR4 reference trace with no PTH connectors is also shown. The frequency response for the above is shown in Figure. 9.




Interpreting results
Figure 9

| Remaining Stub | Delta from Reference | |
|---|---|---|
| | 1.5 GHz | 3.1 GHz |
| .090 | 1.2 dB | 7 dB |
| .220 | .5 dB | 1.2 dB |

For 3.125 Gb/s, the delta between the FR4 reference trace and the .090" stub is 0.5 db at 1.5 Ghz. This deviation from reference is 1.2 db for the .220" stub. Over a band of 50 Mhz to 3Ghz, the maximum attenuation of a .090" stub 1.2 db and the .220" stub is 7 db. Comparing measurements in the time domain for these cases, we see that the .220" stub has had a noticeable effect on the measured eye diagrams shown in Figure 10.

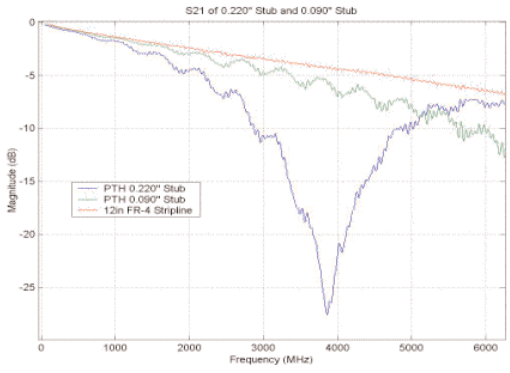


0.220" Stub, jitter 67ps
amplitude = 336mV

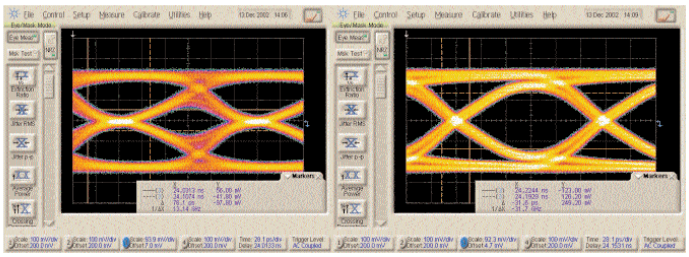
0.090" Stub, jitter = 22ps
amplitude = 327mV

3.125 Eye Patterns
Figure 10

For a 6 Gb/s data stream the fundamental frequency is 3 GHZ , at 3 GHZ the difference between the reference trace and the .090" stub is still 1.2 db and 7 db for the .220" stub. The maximum attenuation of the .090" stub is 3 db and the maximum attenuation of the .220" stub is 27 db for the band of 50 MHz to 6 GHz ( 2 times the fundamental or 6 Ghz.) The notch frequency is now within this band so severe degradation could be expected in the received eye. Measured eye patterns shown in Figure 11 show this effect.




| Remaining Stub | Delta from reference | |
|---|---|---|
| | 3.0 GHz | 6.0 GHz |
| .090<br>.220 | 3.0 db<br>.7 db | 3 db<br>27 db |



0.220" Stub, Jitter76pS, Amplitude 97mV 0.090" Stub, Jitter 31pS, Amplitude 350mV

6.0 Gb/s Eye Pattern
Figure 11

### Bare Board Fabrication Process

Back drilling or controlled depth counter boring is a process where plating is removed from the unused portion of the via multi layer printed wiring boards are processed in a standard manner adding a secondary drilling operation after plating, using PWB CNC drilling equipment with controlled depth enhancements. CNC drill files created from customer data allow this process to be automated and repeatable.

Over Drill Diameter: One important parameter is the secondary drill diameter. This drill diameter must be greater in diameter than the primary drill to allow removal of all the electrodeposited plated metal, typically copper with an additional surface finish. Minimization of this diameter is important to avoid reduction of routing channels which compromise hole to trace spacing in the pin fields. A controlled experiment was done by Teradyne varying the over drill diameter to 5, 7, 10 and 13 mils above original drill size to determine the presence of residual plating. Ten holes from each corner of 4 panels drilled on 4 spindles in one pass were cross-sectioned and evaluated for complete plating removal and internal spacing. No residual plating or spacing violations were observed on any over drill hole size. Teradyne's current recommendation is 7 mils over original drill diameter.

Back drill Depth: Back drilling is a trade off between manufacturing cost and electrical performance. Contributors to back drill depth variation have been characterized which affect yield and cost. Teradyne's optimized setup process achieves a 3 sigma overall variation of +/- 5 mils to nominal target depth. This comes from two components: Mechanical depth and Layer position. It is recommended that at least a 10mil target nominal depth before the last layer connected.

| Attribute | Connector Type | |
|---|---|---|
| | VHDM or VHDM-HSD | GbX |
| Drilled Hole Size | 0.026 | 0.0225 |
| Recommended Back Drill Diameter | 0.033 | 0.0292 |
| Power/Ground Plane Antipad | 0.052 | 0.046 |
| Nominal Spacing Plane to BD Hole Edge | 0.013 | 0.012 |
| Inner Layer Pad Size (1 oz. Cu, 1 mil A/R) | 0.038 | 0.035 |
| Non Back Drilled Outer Layer Pad Size | 0.049 | 0.035 |
| Backd Drilled Adjusted Outer Layer Pad | 0.030 | 0.026 |

Note: Values show are typical. Deviations based on design are not uncommom

Conclusion: Target Diameter = 0.007" over drill diameter

**Back drilling Dimensional Configurations**
**Figure 12**

Bare Board Reliability Testing: A forced failure designed experiment was conducted, intentionally varying process parameters, which took the PTH integrity to extremes. Parameters varied were Drill Hole Quality, Electroless Copper etch back Rate, and Copper Plating Thickness. Test vehicles were subjected to thermal cycling and 6 x solder shock testing. As expected, no failures were observed on either normal PTH's or back drilled PTH's on boards processed under standard conditions. Failures due to cracking were observed on both hole types exhibiting poor drilled hole quality and thin copper plating conditions.

| Variable | Set Point | |
|---|---|---|
| Plated Copper Thickness | High | Low |
| Drilled Hole Quality | Smooth | Rough |
| Etch Back | Positive | Negative |

**Design of Experiment**
**Figure 13**

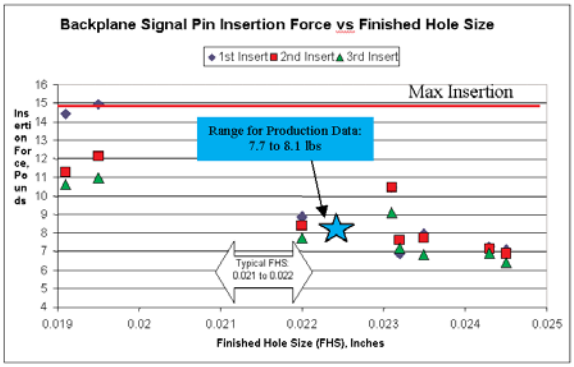



Figure 14A

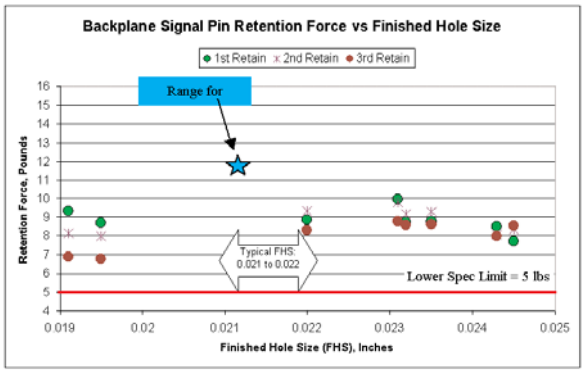



Figure 14B

Cost Model: A cost model developed at Teradyne factors in set up time, run time, and drill bit cost. Application of this model to various board designs results in an average increase of 7 % added to the bare board price. For example, a typical board requiring fifteen hundred back drilled holes would result in an additional cost of about $50 per board.

**Back Drilling Costing Example**

| Attribute | Example 1 | Example 2 | Example 3 |
|---|---|---|---|
| PWB thickness | 0.250 | 0.300 | 0.350 |
| Layer count | 20 | 30 | 40 |
| Depth 1 / Hole Count | 500 | 1000 | 3000 |
| Depth 2 / Hole Count | 0 | 500 | 2000 |
| Depth 3 / Hole Count | 0 | 0 | 1000 |
| Rough PWB price | $500 | $750 | $1,500 |
| Back drilling Charge $ | $30 | $50 | $140 |
| Back drilling Cost Increase % | 6% | 7% | 9% |

**Assuming all boards are FR4 material**

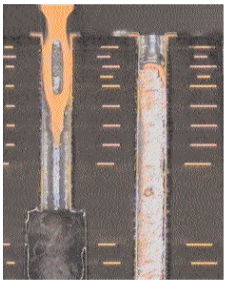
**Figure 15**

### Surface Finishes and Exposed Cu

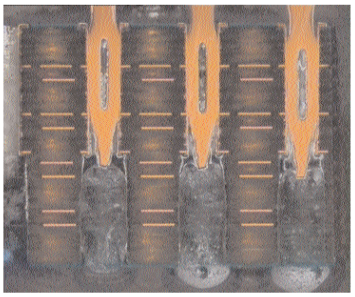
- For Electrolytic Deposited Surface Finishes (re-flowed PbSn, Gold) TCS currently would perform back drilling after that process resulting in exposed copper at the end of the stub.
- Back drilling can be done before Immersion Surface Finishes resulting in no exposed bare copper at the end of the stub.
- Immersion Tin for Back drilled backplanes is preferred.

### Assembly Level Reliability Verification Testing

To evaluate back drilled via structures various reliability testing sequences applicable to PCB vias were performed in accordance with the Telcordia GR-1217-Core and GR-2969-Core requirements for telecommunication hardware. The test plan includes bare board sequences and testing to evaluate press fit termination. This testing has been performed to quality level III. In addition, to the reliability testing, temperature rise and solder shock testing was also performed. Via's were evaluated both with and without anchoring pads at the bottom of the plated hole or back drilled end of the via. See Figure 17 for test vehicle layout.

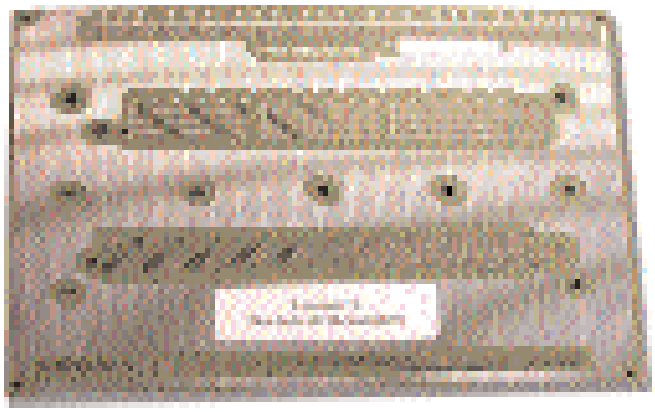


Sample Cross Section without anchor pad



Sample Cross Section with anchor pad

Figure 16



**Telcordia Group 6 Test Vehicle**

**Hole sizes: 0.018" and 0.022"**

**Thickness: 0.260"**

**Layers: 26**

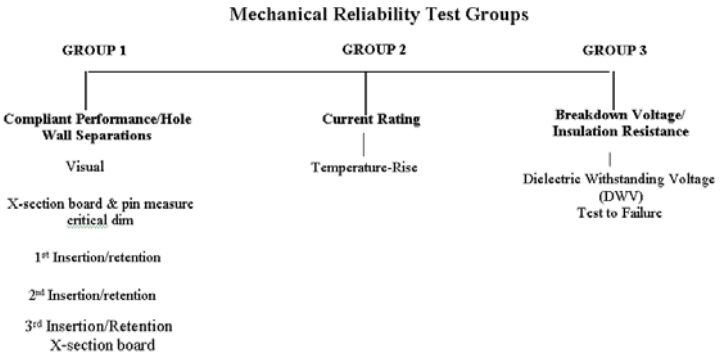
**Material: FR4**

**Size: 8" x 10"**

**Figure 17**

The following reliability test groups were chosen to assess the plated through hole integrity: 1.) Compliant Pin Performance, 3.) DWV dielectric withstanding voltage. 2.) Current Rating, 4-6) humidity cycling and thermal shock, 7.) Mixed flowing gas, 8.) Electro-migration,. The humidity cycling and thermal shock group was chosen to evaluate the effects of thermally stressing the via structure, in order to look for de-lamination between the copper plating and the drilled hole. The mixed flowing gas group was performed to accelerate the corrosion rate between the compliant pin interface and the plated through hole. The purpose of the electro-migration group was to analyze the metallic material growth between the plated through hole and the

exposed copper layers. The compliant pin performance testing was performed to mechanically stress the via structure and to evaluate the performance of the compliant pin. The purpose of mechanically stressing the via structure was to see if the copper hole would de-laminate from the drilled hole wall. A portion of that particular group was also tested to failure, meaning that the pins were purposely pushed through the hole to try to cause the copper to de-laminate. Since back drilling removes copper from the via, the current rating of the via was also tested to evaluate the current capacity. All of the test vehicles had two different via structure, one with anchoring pads and the other without anchoring pads to evaluate the mechanical stability of the via structure. Groups 1 and 4 -6 also had three compliant pin repairs prior to submitting to testing. Below are the results of the testing:




## X-section board

### Group 1 Results: Compliant Pin Insertion - Retention

- Compliant pin performance testing showed no adverse effects on the back drilled hole after 3 insertions and retentions.
- 88 insertion data points
- 66 retention data points

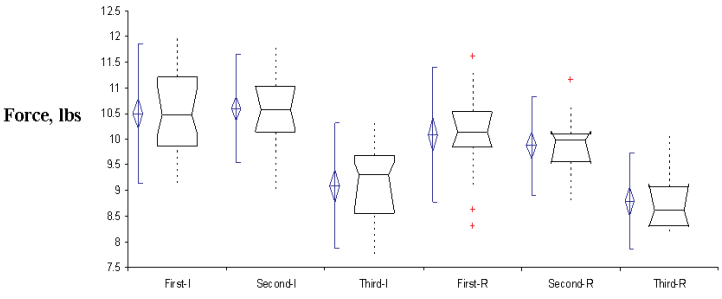


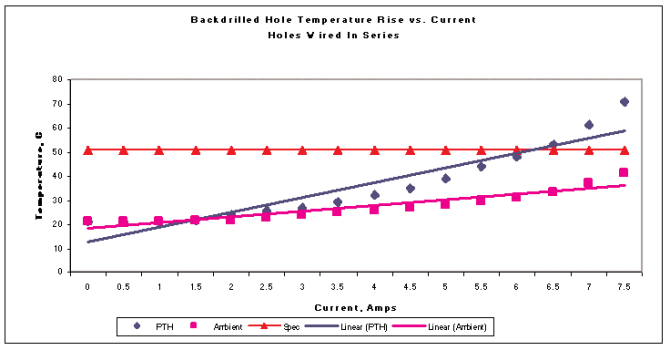

Figure 18, compliant pin insertion – retention force

**Compliant pin insertion - retention force**

**Temperature Rise**

**Figure 19**

### Group 2 Results: Temperature RiseGroup 7 Results: Mixed Flow Gas

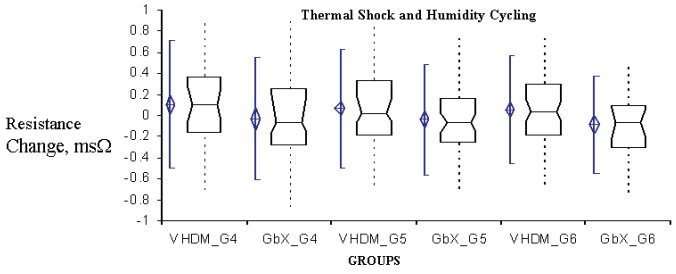



### Reliability Test Plan

**Thermal Shock and Humidity Cycling per GR-1217 Core**

| GROUP 4 | GROUP 5 | GROUP 6 |
|---|---|---|
| *Humidity Cycling & Thermal Shock | *Humidity Cycling & Thermal Shock | *Humidity Cycling & Thermal Shock |
| Visual | Second Insertion Record Force | Third Insertion Record Force |
| LLCR | Visual | Visual |
| Thermal shock –55°C – 85°C 100 cycles | LLCR | LLCR |
| LLCR | Thermal shock –55°C – 85°C 100 cycles | Thermal shock –55°C – 85°C 100 cycles |
| Humidity, cycle 25°C to 65°C 90 to 95%, 50 cycles | LLCR | LLCR |
| LLCR | Humidity, cycle 25°C to 65°C 90 to 95%, 50 cycles | Humidity, cycle 25°C to 65°C 90 to 95%, 50 cycles |
| Thermal shock –55°C – 85°C 100 cycles | LLCR, | LLCR |
| LLCR | Thermal shock –55°C – 85°C 100 cycles | Thermal shock –55°C – 85°C 100 cycles |
| | LLCR | LLCR |

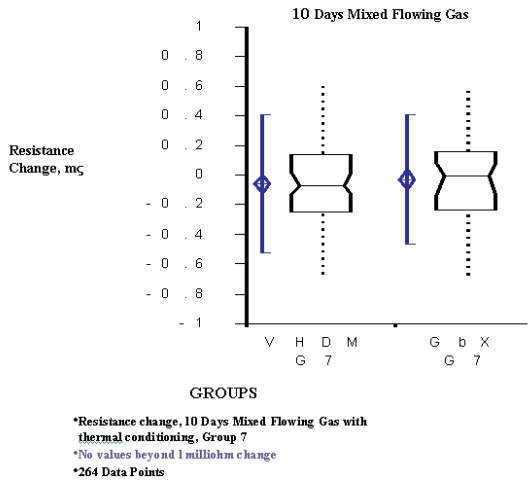
### Group 4 - 6 Results




- Resistance change, Thermal Shock and Humidity Cycling, Groups 4-6
- Group 4- First Insertion
- Group 5- Second Insertion
- Group 6- Third Insertion
- No values beyond 1milliohm change
- 650 Data Points

| GROUP 7 | GROUP 8 | GROUP 9 |
|---|---|---|
| 10 day MFG with & without Pin copper corrosion | Electro-migration | Teradyne Additional Testing |
| Visual | Condition Samples at 65°C and 85% Humidity | |
| LLCR | IR using 45 to 100 Vdc Between Specified Terminals | |
| Thermal condition (300 hrs @ 105°C) | Apply 10Vdc for 500 Hrs At Specified Terminals | |
| LLC | IR using 45 to 100 Vdc Between Specified Terminals | |
| 5 days | | |
| LLCR | | |
| 5 days | | |
| LLCR | | |

### Group 7 Results: Mixed Flowing Gas




Flowing 21, Mixed flowing gas

### Electro-Migration Results

- 500 hours, 10 volt bias
- Spec. requirement: Bellcore 1000 MOhms Minimum
- Results: 15,000 MOhms

As shown, all groups passed testing per stated requirements. The groups all passed without the previously mentioned anchor pads. Group 9 also passed although the intent for these configuration was to stress the hole and not to imply this configuration be used in application.

### Group 9 Results: Additional

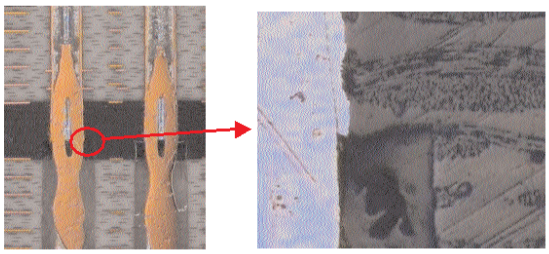
- Solder shock per IPC-TM-650
- Over pinning
- Reverse pinning

Over pinning, no damage observed

No evidence of delamination at the interface of plate hole and back drilled hole

**Figure 22**

Destructive testing, no damage observed



No evidence of delamination at the interface of plated hole and back drilled hole

**Figure 23**

### Conclusions:

The technique of back drilling is being used in production today to tune the characteristics of a plated through hole in a printed circuit board. The decision of when to back drill depends primarily on the signal frequency content and the length of the stub.

Although efforts to reduce stub effect can be accomplished through various techniques such as using lower dielectric material to reduce thickness or routing high speed signals to the bottom of the board, eventually higher frequency designs and increased board thickness will force some treatment of the stub. It is also important to remember that the package or connector is critical to the signal path but independent of the stub effect, and for this reason changing the termination from press fit to SMT may not resolve the inherent stub induced signal loss.

### Summary of Implementation Recommendations

- Optimize pattern
  - Reduce crosstalk in footprint by alternating back drilled vias
  - Match long trace lengths with shortest via stub
- Establish zones to minimize number of back drill depths
- Remove non-functional pads
- Creative routing and netlist design can remove layers and min imize via stub effects by thinnnig the boards

Looking forward, on-going effort will be required on seamless implementation of the design rules, evaluating the electrical and reliability effects of plated through hole used in an SMT application, and further refining the design rules based on other structures.

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**References:**

Transmission Line Design Handbook - Brian Wadell

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