High Performance Package Trends Driving BackDrill File Generation Using Cadence Allegro

By

Chris Heard and Leigh Eichel

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1. Introduction

As the semiconductor industry passes the 100 billion unit mark for IC shipments in 2004, advanced packaging technologies continue to play an important role in the semiconductor industry's future. The realization of Moore's Law within the "front-end" of semiconductor processing must also be enabled by new methods in the "back-end" of semiconductor packaging. Such technologies include chip scale packages (CSPs), stacked packages, system-in-package (SIP), and technologies aimed at the markets for radio frequency (RF) devices. With all the attention given to wafer processing, IC advances, and microelectronics end products, we tend to lose sight of the fact that IC packaging is also being pushed to a higher level of sophistication. There is an increasing demand for high-level coordination between silicon and package designers much earlier in the new product development sequence. The net result is an unprecedented rate of advanced IC package solutions.

Package proliferation is primarily a response to performance demands being placed on the package by the continuous evolution of semiconductor device and end-product system technology. On the device side, smaller lithography, higher operating frequency, higher power dissipation, and increasing numbers of interconnects to other components all lead to continuously evolving package structures and assembly technology. Thinner, smaller end-products with increasing functionality also create challenges for existing packaging. If cost could be ignored, it is likely that a small number of package structures could adequately support all these device and system level requirements. Given the extreme cost pressure throughout most of the electronics supply chain, however, package solutions that offer just the right level of performance at the lowest cost will continue

Today, most package proliferation can be attributed to technical and cost demands placed on the package by device and system engineers. Along with increasingly complex package selection decisions, electronic component manufacturers also face difficult decisions about which functional blocks of a system should be partitioned into an individual package in the first place. System level integration in an IC package (system in a package, SiP) is fast becoming the approach of choice for many high-performance and space-sensitive applications.

Tiny packages with high-density I/O and ultra-narrow pin spacing create two types of engineering problems: One is the increased probability of noise, crosstalk and signal integrity issues. Narrow pin-spacing between high-speed signal lines increase crosstalk and narrow trace widths increase loss. This increase in noise can result in false logic triggers through the threshold region on single ended nets and excessive jitter on differential nets. Often, the result is a decrease in data transmission rates or an increase in power consumption, as the receiver circuitry must utilize more complex equalization techniques to successfully extract a digital event.

The following 3 charts illustrate the trends in IC packaging which by most accounts will continue and thus put even more pressure on full system engineering, Design for Manufacturing (DFx) automation and total product life cycle cost analysis.

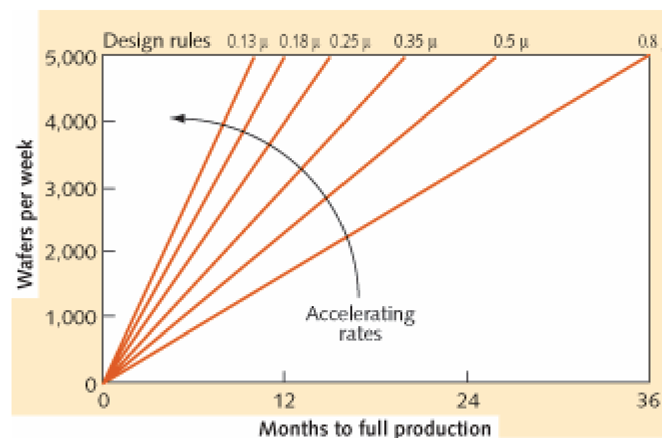


Figure 1. Rate of fab ramp-up to full production. (Source: Rose Associates, IC Insights)

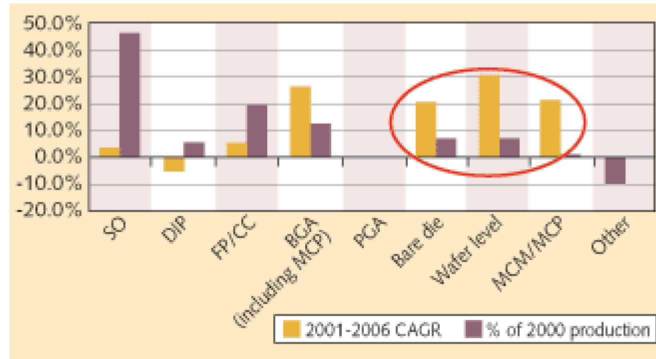
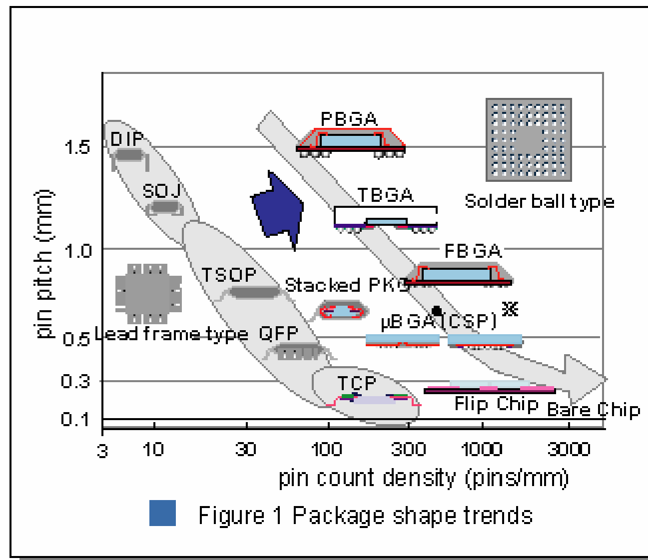


Figure 2. Compounded annual growth rate (CAGR) of different packaging formats. (Source: TechSearch International, IC Insights)



*µBGA is a registered trademark of Tessera Inc., USA.

Figure 3. Different packaging formats vs. density and pin I/O. (Source: Hitachi)

The Cascading Engineering Effect

The trends above drive a cascade of continuous engineering development work with much more complex printed daughter card and backplane circuit board designs. These designs require the most advanced techniques in layout. The issue is not only fine-pitch routing; it is also in multiplayer printed circuit manufacturing via formation. These devices have such a high pin count that leaves very few options in terms of methods to increase the number of routing channels and pin escapes. This puts pressure on the number of layers used and or the methods to form the interconnect using techniques such as via in pad, sequential lamination or stacked vias. Generally, the number of high performance circuit layers must be roughly equivalent to the number of pin-rows on your BGA to ensure that all signals lines have can be properly routed. Larger BGAs in excess of 1500 pins and 0.8mm ball pitch can end up dominating the total routing effort.

New generations of ICs are communicating at ever-higher data rates. I/O speeds from 6.25Gb/s and faster are becoming more prevalent. As I/O speeds increase, package and PCB discontinuities become hindrances to interconnecting these high-speed devices. Thus, like SoC design, IC packaging is thrown into an early alliance with EDA tools in an effort to understand the signal integrity penalties imposed by high-density, high-pin counts and high speeds on one hand, and to affect an ultra-precise printed circuit board layout and trace routing on the other.

The Need to Backdrill vias

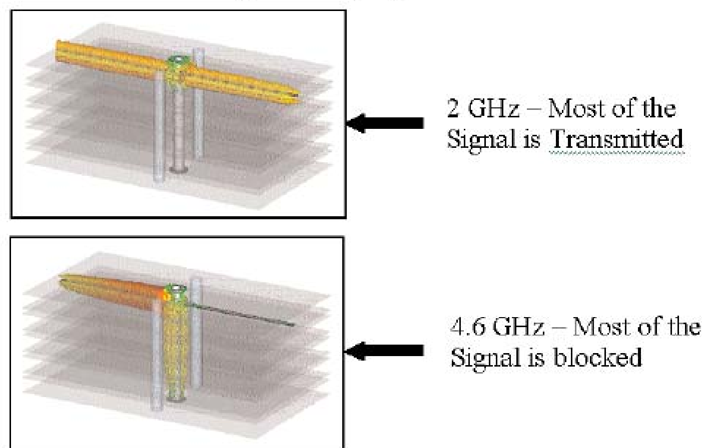
Many systems contain several circuits and high reliability board-to-board interconnects. Thus the massive amount of I/O creates further challenges. One of the challenges that is becoming much more common is the need to back drill backplanes to ensure the highest fidelity signals can be carried at ever increasing speeds.

Transport data rates of 3.125 Gb/s are now commonplace in board-to board applications. As data rates increase to 5, 6.25 or 10 Gb/s the entire channel topography will need to be re-examined. A typical transmission channel includes signal traces, connectors, and plated through hole vias. New connectors are entering the market with better impedance matching and improved shielding techniques to accommodate the sharper rise times associated with the faster data rates. Likewise laminate suppliers continue to develop new board materials with lower loss tangents to reduce the signal attenuation due to laminate loss. Using equalization circuits and signal pre-emphasis, device suppliers are driving solutions to improve signal fidelity at increased data rates, thereby extending the use of conventional laminate materials.

A piece of the transmission path which has become a dominant effect, is the plated through hole or via. Plated through holes or PTH's are a means to transport signals into interior layers of a multi layer PC board. PTH vias are used in this way under the pad array of the device package, and in the launch of separable connector interface into boards. The PTH is common to various device packages such as a ball grid array (BGA) and connector types including press fit and surface mount right angle board-to-board, mezzanine and cable connectors.

The PTH portion of the signal path becomes more "visible" to the signal as increased frequency content is needed to produce sharp rise and fall times of the digital pulse. The focus of this paper will be on a technique commonly referred to as back drilling or counter boring of the printed circuit board PTH. Included in this study will be the electrical effect, the process implications including a cost model and results of long term reliability testing.

The actual rise time and frequency content of digital pulses may vary. The frequency spectrum of a PRBS digital data stream typically consists of bands centered around a fundamental and its odd harmonics. The fundamental frequency of the spectrum occurs at one half of the data rate. At 6.25Gbits/sec, this means that the fundamental frequency would occur around 3.125GHz with some contribution around the third (9.38 GHz) and fifth (15.25GHz) harmonics. A PTH or through via joining a surface pad or connector to an inner layer strip line trace, can behave as a parasitic element or transmission line discontinuity. It acts as a notch filter centered around a frequency primarily determined by the unused portion of the hole, sometimes referred to as a resonant stub. As a signal transitions into a plated through hole, some of the energy is reflected back to the source from the impedance discontinuity. The remaining energy proceeds through the via. The energy that is transitioning through the plated through hole uses the hole as a transmission line element whose parameters are defined by the physical dimensions of the structure (pad size, anti-pad size, thickness, material, etc.) It then reaches an impedance matched stripline layer. Some of the energy is transmitted into this layer and some continues to travel down the remaining via. Any portion of the plated through hole below the exiting stripline layer can be looked at as an open transmission element referred to as a stub.



Vias Stubs Cause High Speed Signals to Resonate

Bare Board Fabrication Process
Back drilling or controlled depth counter boring is a process where plating is removed from the unused portion of the via. Multi layer printed wiring boards are processed in a standard manner adding a secondary drilling operation after plating, using PWB CNC drilling equipment with controlled depth enhancements. CNC drill files created from customer data allow this process to be automated and repeatable.

Over Drill Diameter: One important parameter is the secondary drill diameter. This drill diameter must be greater in diameter than the primary drill to allow removal of all the electrodeposited plated metal, typically copper with an additional surface finish. Minimization of this diameter is important to avoid reduction of routing channels which compromise hole to trace spacing in the pin fields. A controlled experiment was done by Teradyne varying the over drill diameter to 5, 7, 10 and 13 mils above original drill size to determine the presence of residual plating. Ten holes from each corner of 4 panels drilled on 4 spindles in one pass were cross-sectioned and evaluated for complete plating removal and internal spacing. No residual plating or spacing violations were observed on any over drill hole size. Teradyne's current recommendation is 7 mils over original drill diameter.

The method to create all the necessary information to create files required for backdrilling using Cadence Allegro 15.x and greater follows:

Description of the Back Drilling Deliverables

When post processing of a pcb design is done, an ncdrill.tap file is created. The ncdrill.tap file contains an “Excellon formatted” list of every location on the backplane that is drilled. It also contains the tools (drill sizes) for each location. Of course, the assumption is that the drill goes through the entire thickness of the board at every location.

Backdrilling is a secondary operation that removes the plating in a hole from a certain side to a certain depth. An Excellon formatted list of locations per side per depth is required.

Cadence Allegro has a report generation utility called “extracta”. Extracta requires an input text file called a “view file” and generates a report. This document will describe how to create the view file.

Once the output file is generated, it needs to be read into an available Excel file in order to 1) Decide which nets get backdrilled and 2) Format the locations in Excellon Format.

Once the data is formatted properly, it can be copied and pasted into a separate ASCII text drill file.

Step 1: Determine Minimum Stub

Stackup details, signal frequency of operation and dielectric constant of material determine how many depths are required. The following table describes how to calculate minimum stub length at a given frequency of operation.

Data Rate	6.25 Gb/S	
Nyquist Frequency	3.125 GHz	Data Rate / 2
Stub Frequency	9.375 GHz	Nyquist Frequency * 3
¼ Wave Propagation Delay	22 pS	(1/(4* Stub Freq))/1.2
Dielectric Prop Delay	174 pS/in	84.7*(sqrt(Er)), Er = 4.2 for FR4
Minimum Stub	0.128”	¼ Wave Delay / Prop Delay

Table: Minimum Stub Calculation

Once the minimum stub is calculated, determine the number of depths and the layers that pertain to each depth in the stackup.

Step 2: Determine Number of Depths

In the following stackup, using 0.128” as a guideline for minimum stub depth, a table of depths and associated layers is developed.

	Dielectric	Copper	Stub w/No Backdrilling	Depth Number	Stub w/ Backdrilling
Layer 1	0.009	0.0012			
Layer 2	0.009	0.0012			
Layer 3	0.009	0.0006	0.190	1	0.079
Layer 4	0.009	0.0012			
Layer 5	0.009	0.0006	0.170	1	0.070
Layer 6	0.009	0.0012			
Layer 7	0.009	0.0006	0.151	1	0.050
Layer 8	0.009	0.0012			
Layer 9	0.009	0.0006	0.131		0.030
Layer 10	0.009	0.0012			
Layer 11	0.009	0.0012			
Layer 12	0.009	0.0012			
Layer 13	0.009	0.0012			
Layer 14	0.009	0.0006	0.080		
Layer 15	0.009	0.0012			
Layer 16	0.009	0.0006	0.061		
Layer 17	0.009	0.0012			
Layer 18	0.009	0.0006	0.041		
Layer 19	0.009	0.0012			
Layer 20	0.009	0.0006	0.021		
Layer 21	0.009	0.0012			
Layer 22		0.0012			
Total Thickness	0.211				

BD 1 Depth

Stub Calculations

Only one depth ("BD1") is required in order to keep all the stubs below 0.128". For this design, a single depth up to but not including layer 11 will be used.

Step 3: Create the "View File"

The Allegro board file refers to layers as "L3" in this example. The following is a view file that creates a report for Layers 3, 5 7, and 9 for components mounted on the top side of the board. For components on the top side of the board, set SYM_MIRROR = No. For components on the bottom side of the board, set SYM_MIRROR = Yes.

```
*********Start of File******************
FULL_GEOMETRY

# FILTERS FOR EACH FILE:

        CLASS = 'PIN'
        PAD_CONNECTED = 'YES'
        SYM_MIRROR = NO
        SUBCLASS = L3
        DRILL_HOLE_NAME != ''
                OR
        CLASS = 'PIN'
        PAD_CONNECTED = 'YES'
        SYM_MIRROR = NO
        SUBCLASS = L5
        DRILL_HOLE_NAME != ''
                OR
        CLASS = 'PIN'
        PAD_CONNECTED = 'YES'
        SYM_MIRROR = NO
        SUBCLASS = L7
```

DRILL_HOLE_NAME != ''
OR
CLASS = 'PIN'
PAD_CONNECTED = 'YES'
SYM_MIRROR = NO
SUBCLASS = L9
DRILL_HOLE_NAME != ''

OUTPUT DATA:

NET_NAME
SUBCLASS
REFDES
PIN_NUMBER
DRILL_HOLE_NAME
DRILL_HOLE_X
DRILL_HOLE_Y
*********End of File*****************
Copy the text after the "Start of File" line and before the "End of File" line and paste it into an ASCII text file called "pads_top_lyr3579.txt"

Step 4: Run the Extracta Command.

Start a DOS window (also called a Command Prompt). Navigate to the directory where the .brd file is located. Enter the following command where "teradyne_bp" is the name of the .brd file:

extracta teradyne_bp pads_top_lyr3579 pads_top_lyr3579_out

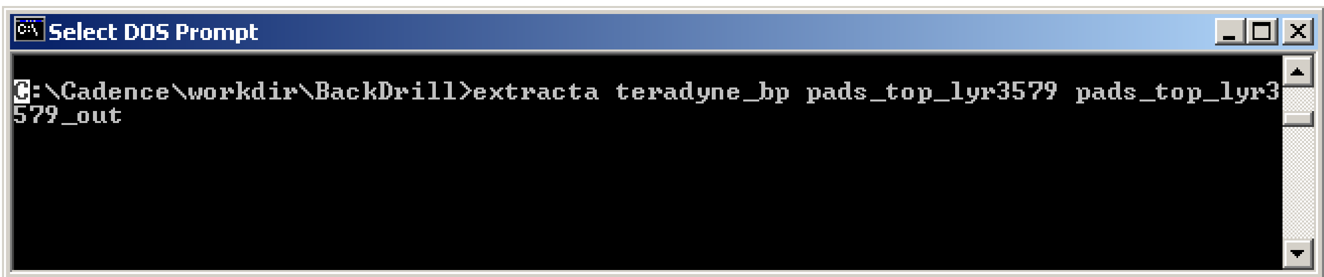


Figure: Extracta Command

Every pad location on the board gets read. Extracta reports back on whether the hole is connected to either of the 4 layers. The final window looks like this:

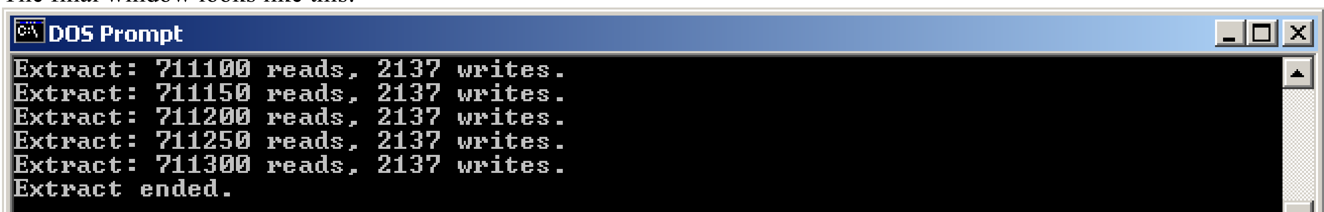


Figure: Extracta Command Results

2137 pad locations have been found on the four layers in question.

2. Step 5: Remove Nets From Report

Extracta reports on ALL the holes connected to the 4 layers. In many designs, not all of these locations are high speed nets. Thankfully, the report is sorted by net name so it is easy to remove low speed nets based on net name. After removal of low speed nets, the report now looks like this:

A!NET_NAME!SUBCLASS!REFDES!PIN_NUMBER!DRILL_HOLE_NAME!DRILL_HOLE_X!DRILL_HOLE_Y!
S!DP996P!L7!J59!P5!18.00!29149.70!-13457.76!
S!DP996N!L7!J59!Q5!18.00!29212.69!-13394.77!
S!DP995P!L7!J59!P4!18.00!29149.70!-13615.24!
S!DP995N!L7!J59!Q4!18.00!29212.69!-13552.25!
S!DP994P!L3!J59!P3!18.00!29149.70!-13772.72!
S!DP994N!L3!J59!Q3!18.00!29212.69!-13709.73!

DP996P and DP996N are positive and negative nets comprising a differential pair and are representative of nets that should be backdrilled.

Step 6: Read Text File Into Excel and Format Excellon Data

Using the exclamation point as the text delimiter, the text file can be opened directly into Excel and the data then copied and pasted into a sheet that concatenates the appropriate X and Y locations into Excellon format:

A	NET_NAME	SUBCLASS	REFDES	PIN_NUMBEF	DRILL_HOLE	DRILL_HOLE	DRILL_HOLE_Y			Excellon Callout
S	DP996P	L7	J59	P5	18	29149.7	-13457.76			
S	DP996N	L7	J59	Q5	18	29212.69	-13394.77	00029213	-00013395	X00029213Y-00013395
S	DP995P	L7	J59	P4	18	29149.7	-13615.24	00029150	-00013615	X00029150Y-00013615
S	DP995N	L7	J59	Q4	18	29212.69	-13552.25	00029213	-00013552	X00029213Y-00013552
S	DP994P	L7	J59	P3	18	29149.7	-13772.72	00029150	-00013773	X00029150Y-00013773
S	DP994N	L7	J59	Q3	18	29212.69	-13709.73	00029213	-00013710	X00029213Y-00013710
S	DP993P	L7	J59	P2	18	29149.7	-13930.2	00029150	-00013930	X00029150Y-00013930
S	DP993N	L7	J59	Q2	18	29212.69	-13867.21	00029213	-00013867	X00029213Y-00013867

Table: Excellon Format Concatenation

The last column in the chart is the Excellon formatted data is is generated by the following Excel formula: =CONCATENATE("X",TEXT(I3,"00000000"),"Y",TEXT(J3,"00000000")).

Step 7: Create Separate Drill File

Copy the last column in the chart under "Excellon Callout" and paste the text data into a separate text file. Name the file "1801.tap". The "18" in the file name is the drill diameter and the "01" in the file signifies depth #1. The contents of the file should look like this:

```
;FILE : backdrill file from bottom surface, depth #1 up to but not including L11
;Holesize 1. = 18.000000 PLATED MILS
X-00000108Y-00014088
X00000049Y-00014088
X00000364Y-00014088
X00001467Y-00014088
X00001625Y-00014088
X00002255Y-00014088
X00003200Y-00014088
X00003358Y-00014088
```

Include this file with the standard ncdrill.tap file in whatever .zip file is created for the deliverables.

Step 8: Add Note to Fabrication Drawing

The following note in the fabrication drawing is required to ensure proper handling of the backdrill data:

"Use file 1801.TAP for the locations of backdrilling for layers 3, 5, 7 and 9. Backdrill via to completely remove the copper plating from the bottom layer through layer 12 but not through layer 11."